Final Report on

NASA Grant NSG-3024

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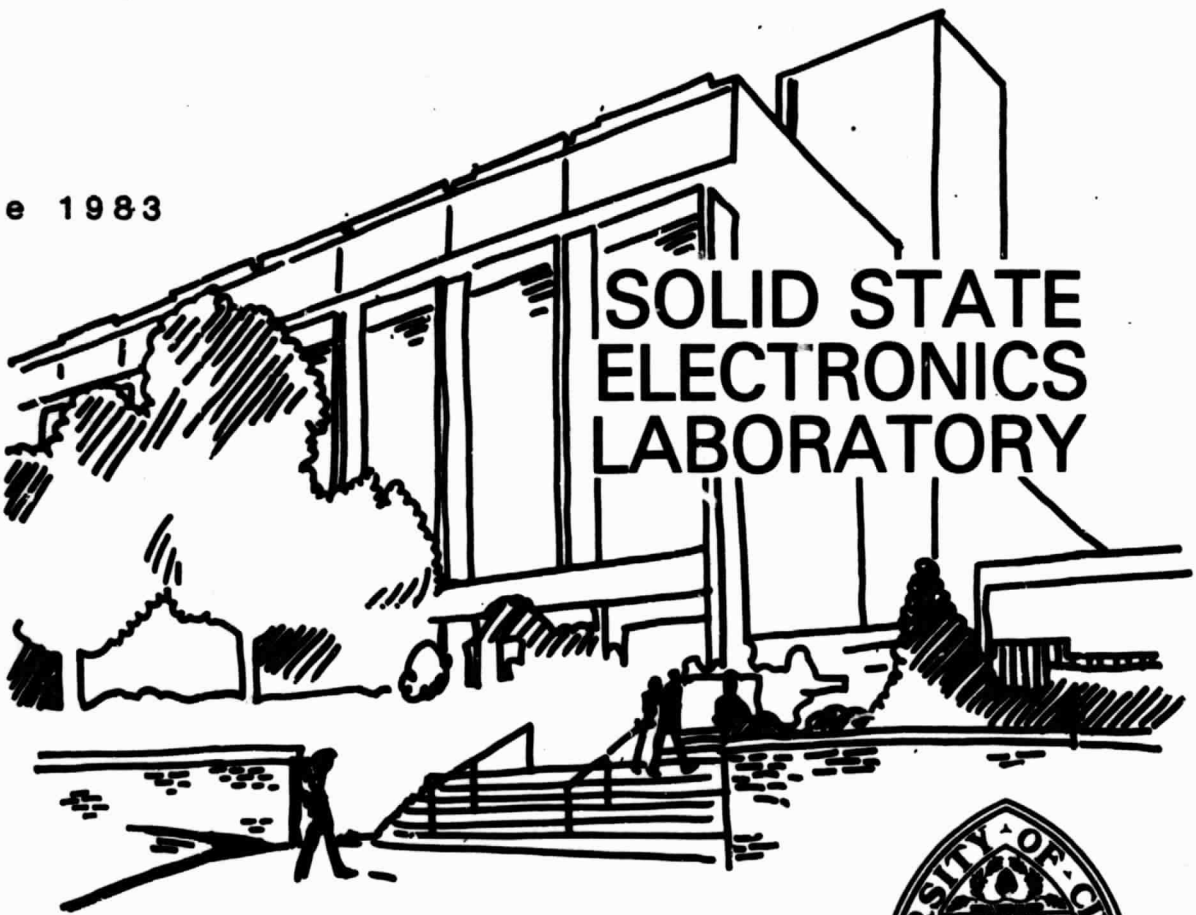
RESEARCH INTO THE USE OF PYROLYTIC OXIDES AND POLYMERS FOR THE FABRICATION OF THIN FILM HIGH ENERGY CAPACITORS

June 1983



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Final Report on

RESEARCH INTO THE USE OF PYROLYTIC OXIDES AND POLYMERS FOR THE FABRICATION OF THIN FILM HIGH ENERGY DENSITY CAPACITORS

NASA Grant NSG-3024

National Aeronautics and Space Administration

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1. SILICON DIOXIDE DIELECTRIC

1.1 INTRODUCTION

The research into the use of silane pyrolytic deposition methods for silicon dioxide growth for the purpose of fabricating high energy density capacitors had two major phases of activity. The first phase, dealt mainly with the construction of single layer capacitors and the evaluation of their properties. By this means, the relative value of the basic approach was studied and the techniques perfected which led then to multiple layer capacitors. The second phase built upon the knowledge gained in the construction of single layer capacitors in order to make multiple layer capacitors. It was in Phase II that efforts were concentrated on such important aspects of the work as total weight and multiple layer bonding considerations. Surface roughness and stress considerations were also an important part of this phase of the research.

1.2 SINGLE LAYER CAPACITORS

1.2.1 Construction

It was obvious from the onset that the quality of the silicon dioxide, which was being used as the capacitor dielectric, would be of paramount importance. The freedom from pin holes and the uniformity of the oxide were the most important features of the oxide after growth. However, in order to establish a fabrication procedure which could be extended to perhaps as many as 100 layers, the rate of oxide growth was also a very important consideration. If the oxide is to be deposited on aluminum electrodes, the temperature of the growth becomes another parameter in the selection of the proper oxide deposition process.

Although several possibilities existed, it appeared that the oxidation of silane at a low temperature had the best potential for satisfying all of the requirements mentioned above. This was the approach originally proposed to NASA and was the approach adopted. The high growth rate and low (400°C) deposition temperature are inherent in the process. As an example, the growth rates attained for the equipment used in this work could be conveniently varied from .02 to .12 μm/min.

The most difficult of the specifications to meet were the ones dealing with the quality of the oxide as reflected in the pin holes and uniformity. Both factors are of concern when the breakdown voltage is taken into consideration because of the rather large (at least $1cm^2$) areas involved. It was these factors which led to the decision to purchase a commercial reactor rather than to build one from scratch.

The reactor selected was a Nav-Tec System 300. Although the specifications indicated that $\pm$6% uniformity was obtainable, it was found that this was not an easily attainable result. Quite a bit of effort was expended and changes made in the reactor in order to achieve the required uniformity. The uniformity achieved was about $\pm$5% across a 2" diameter surface. This is more than adequate for the intended purposes.

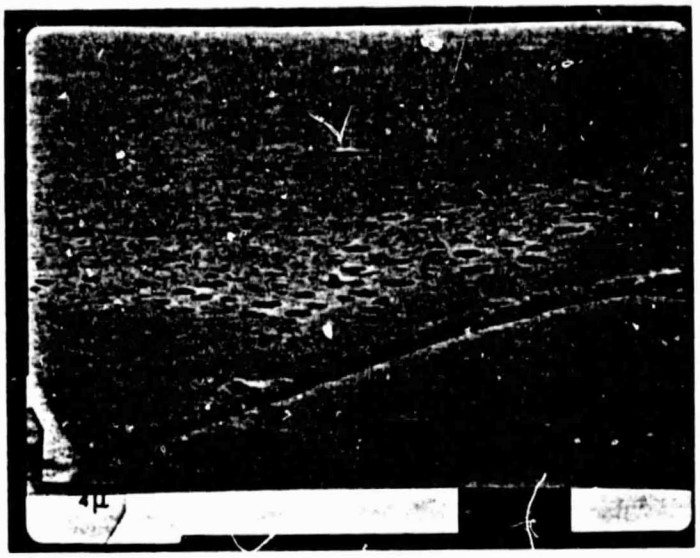
The pin hole size and density play an important role in determining the breakdown voltage of the capacitors. The principal factor is the size of the pin holes. If they are sufficiently small, shorts will not occur when the metal electrodes are applied, because the metal will not tend to fill a very small diameter hole. Even if a short does occur in such a hole, tests have shown that it can be burned out by a short dura-

tion current pulse. Based on comparisons with integrated circuit technology, we have predicted that if the pin hole size and density can be made comparable to that of a thermally grown wet oxide, that satisfactory results will be obtained when capacitors are constructed from such oxides.

Figure 1 shows scanning electron microscope photographs of both thermally grown silicon dioxide and oxide which was pyrolytically deposited in our laboratory. The pictures indicated a pyrolytic oxide quality which is comparable to that of the wet thermal oxide. This evidence coupled with the uniformity measurements indicated clearly that the oxide deposition process is an excellent one and that a rather good control has been achieved. Although quite a bit of time and effort went into setting up the oxide deposition system, it has resulted in high quality oxides.

After obtaining control over the oxide growth process, the next step was the fabrication of single layer capacitors to evaluate the breakdown voltage of the oxide as well as to determine the effective dielectric constant of the oxide.

The capacitors which were initially built were made using the construction technique shown in Fig. 2. The substrate was a silicon wafer, approximately 2" in diameter. The resistivity of the substrate was in the range of 1 to 5 ohm-cm. The wafers were cleaned prior to growth. The cleaning steps were mainly designed to remove particulate contaminants rather than surface adsorbed chemical contamination. Silicon dioxide was grown on the substrate at a temperature of 400°C. The



Wet thermal SiO_2

Approx. 3250 X

Pyrolytic SiO_2

Approx. 3880 X

Pyrolytic SiO_2

Approx. 7500 X

Fig. 1. SEM photographs of thermal and pyrolytic oxides.

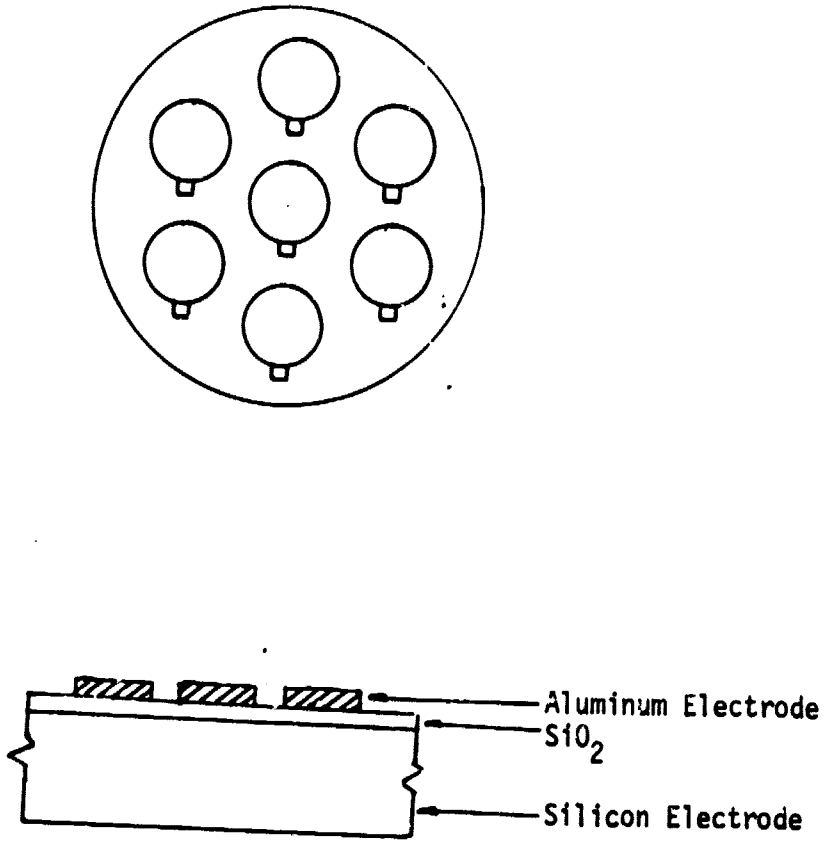


Fig. 2. Capacitor construction.

thickness of the oxide was approximately 1 μm. The top electrode was a circular aluminum plate 1 cm^2 in area. Seven such top electrodes were deposited onto each wafer by evaporation through a mask. The evaporation was performed in a standard evaporator at a pressure of about 10^{-4} to 10^{-5} Torr. The aluminum was evaporated from a tungsten resistance heater.

Each wafer so constructed now had seven capacitors, each of which could be probed and tested independently. Each capacitor had a small tab on the aluminum electrode. The purpose of this tab was to make a connection point for multiple layer capacitors by simply rotating the tab location after each oxide layer was deposited. It had no advantage in the construction of the single layer capacitors.

A large number of such capacitors were made and tested. The initial tests were made to determine which capacitors had been shorted during fabrication. This test could be made by simply using an ohmeter. Occasionally, due to mask alignment errors, one or two of the capacitors were over the edge of the wafer. These were not counted in any of the tests because they, of course, would always be shorted and would yield no useful information. Of the capacitors which were completely within the confines of the wafer area, the percent which were <u>not</u> shorted varied from 60% to 100%. The shorts were due no doubt to pin holes in the oxide. These pin holes were large enough to permit the evaporated aluminum top electrode to contact the silicon substrate. In the initial work no attempt was made to burn out these shorts by the use of high current pulses. This was done in later work however.

The fact that there were some wafers in which no shorts occurred was quite encouraging. This indicated that control of the oxide quality over a wide area was possible. Obviously, for multiple layer capacitors to be achieved, the shorting problem must be controlled even more closely.

1.2.2 Capacitance and Dissipation Factor

The plots of capacitance vs. frequency are shown in Fig. 3. Each plot represents the average capacitance of the capacitors on a particular wafer. The theoretical value for the capacitance, assuming a relative dielectric constant of 4 for the silicon dioxide, is 3540pF. The values measured are within the accuracy range of which the relative dielectric constant of silicon dioxide is known. The differences from one wafer to another were due mainly to the different oxide thicknesses. The capacitance values were measured by using a probe to make contacts to the capacitors and a General Radio Model 1610C capacitance measuring system.

The dissipation factor was also measured as a function of frequency and the average value for the capacitors of each wafer is plotted in Fig. 4. The dissipation factor is due to energy losses both in the dielectric and in the lower silicon electrode. Not until an all aluminum electrode system was constructed, was it possible to accurately separate those two components. Even so, the dissipation factor was not extremely high, although it does increase at higher frequencies. Sample Al-12N was the only one of the group shown in which the oxide was not

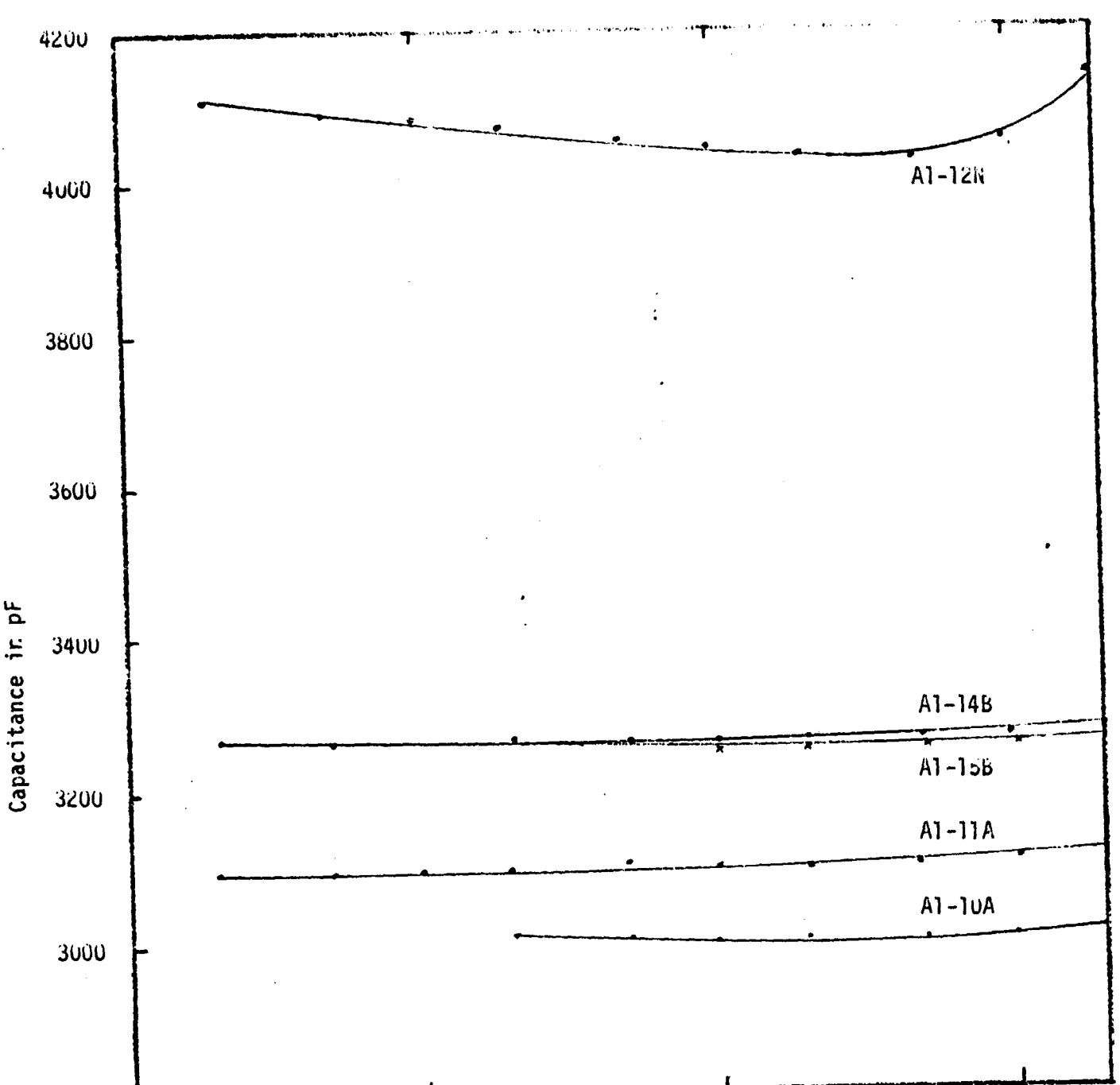


Fig. 3. Capacitance vs. frequency for several sets of capacitors.

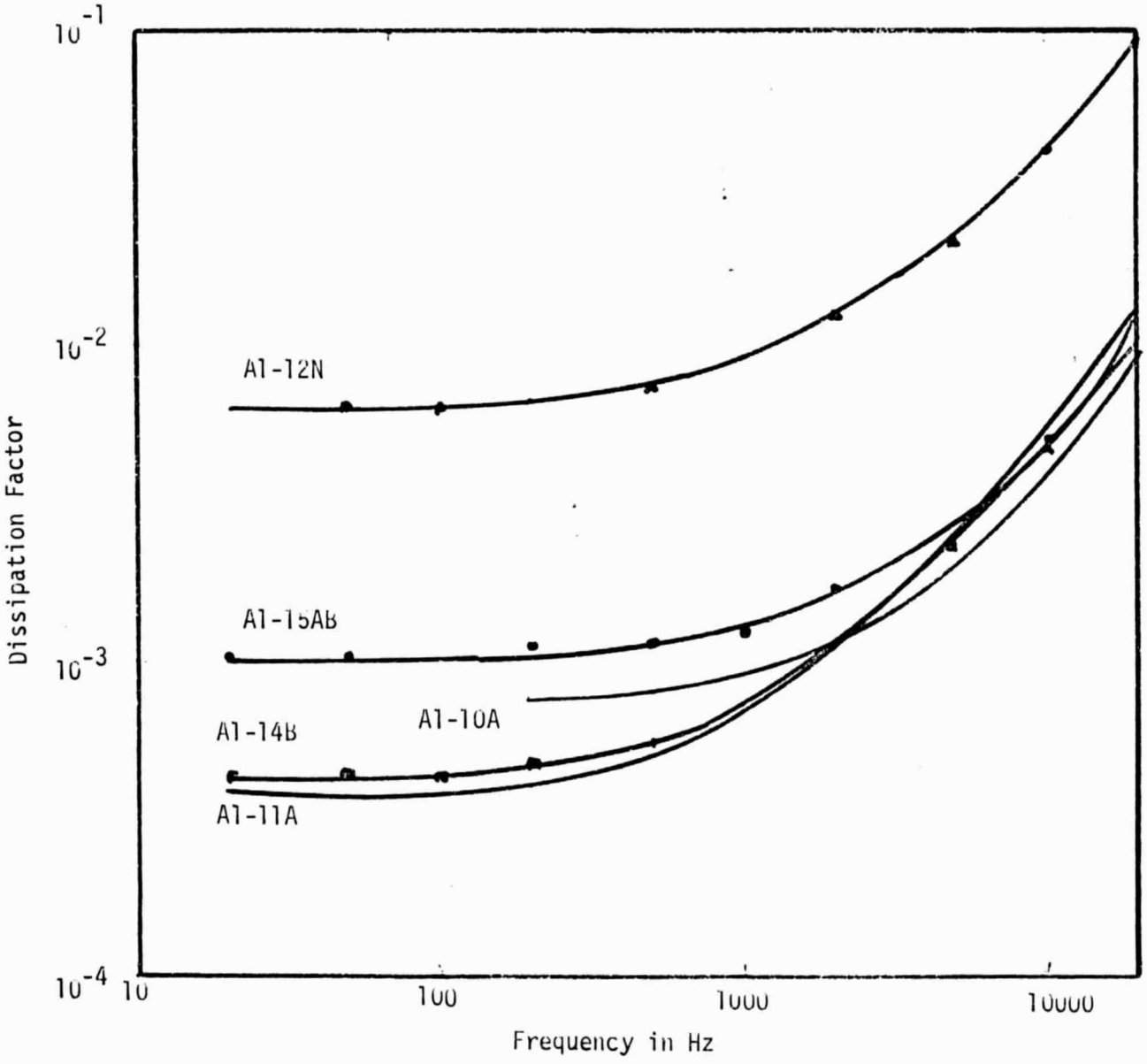


Fig. 4. Dissipation factor vs. frequency for several sets of capacitors.

annealed after growth. The effect on the dissipation factor is quite noticeable. During the growth of the silicon dioxide, a by-product of water is formed and is incorporated into the growing oxide. Annealing drives off most of this water. Apparently, it is this water trapped in the oxide which increases the dissipation factor. One of the conclusions thus reached concerning the oxide growth process was that the annealing step is a necessity if low dissipation factors are desired.

There was some decrease in the dissipation factor when the pyrolytic oxides were annealed at a sufficiently high temperature. This is presumed to be caused by a drive-off of the trapped water or hydrogen. The plot of dissipation factor as a function of anneal temperature is shown in Figure 5. Clearly there is some advantage in annealing the oxides at high temperatures. Unfortunately, the high temperature annealing is not compatible with many of the electrode materials. Thus if annealing is done at all, it must be done at fairly low temperatures (500 ℃ to 600°C) in order to avoid undesirable interaction between the oxide and the electrodes. A particularly sensitive test to determine the degree of densification of the oxide during annealing is the etch rate test. The rate at which pyrolytic oxides etch in a buffered hydrofluoric acid solution is strongly dependent on the annealing time and temperature. Figure 6 is a plot of the etch rate as a function of the annealing temperature for a five minute anneal. The final value of etch rate will approach that of thermal oxides (0.05 to 0.06 μ/min) for longer anneal times.

The breakdown voltage was measured for each capacitor using a simple test system with a power supply and series resistor. The supply

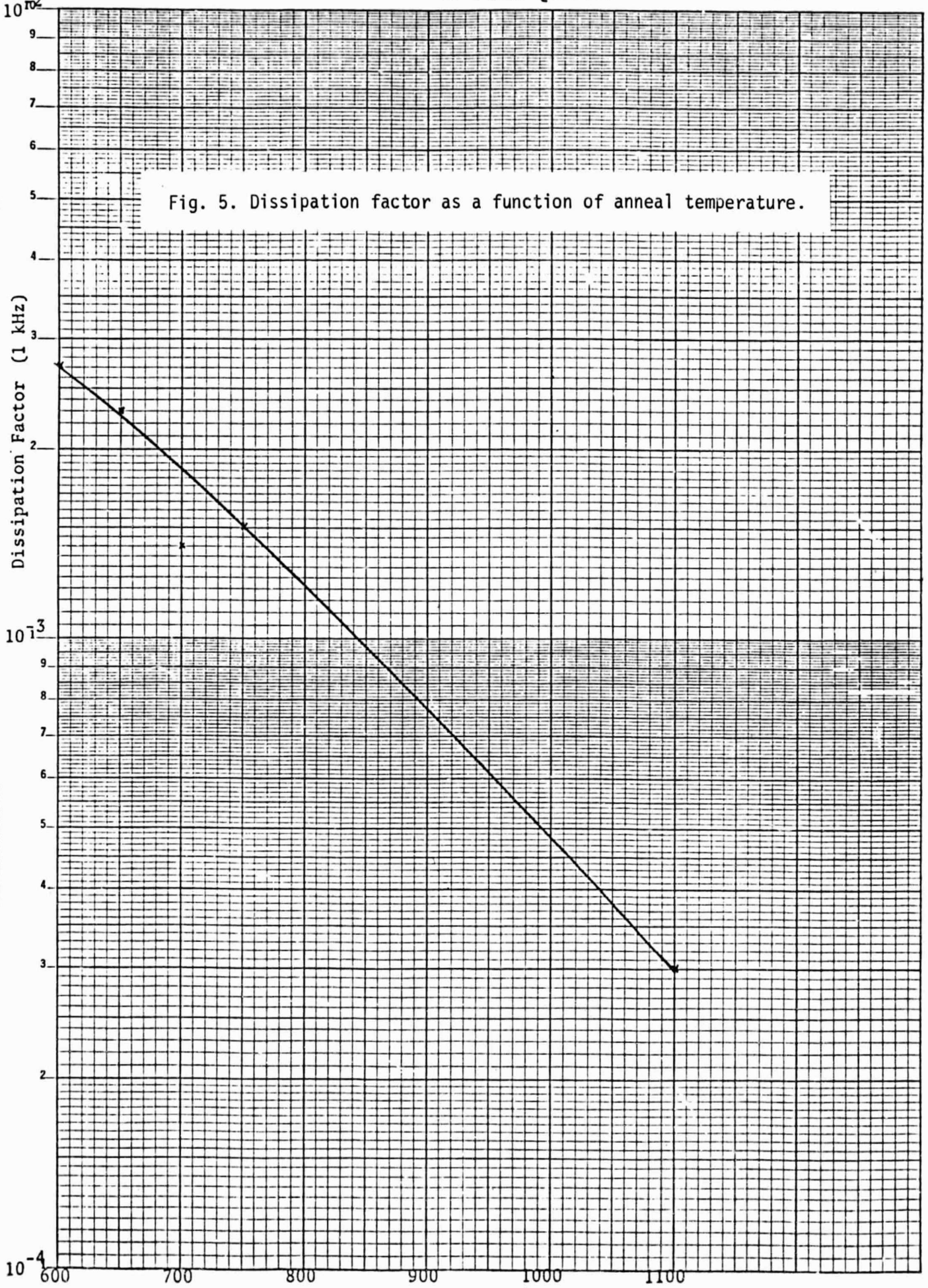
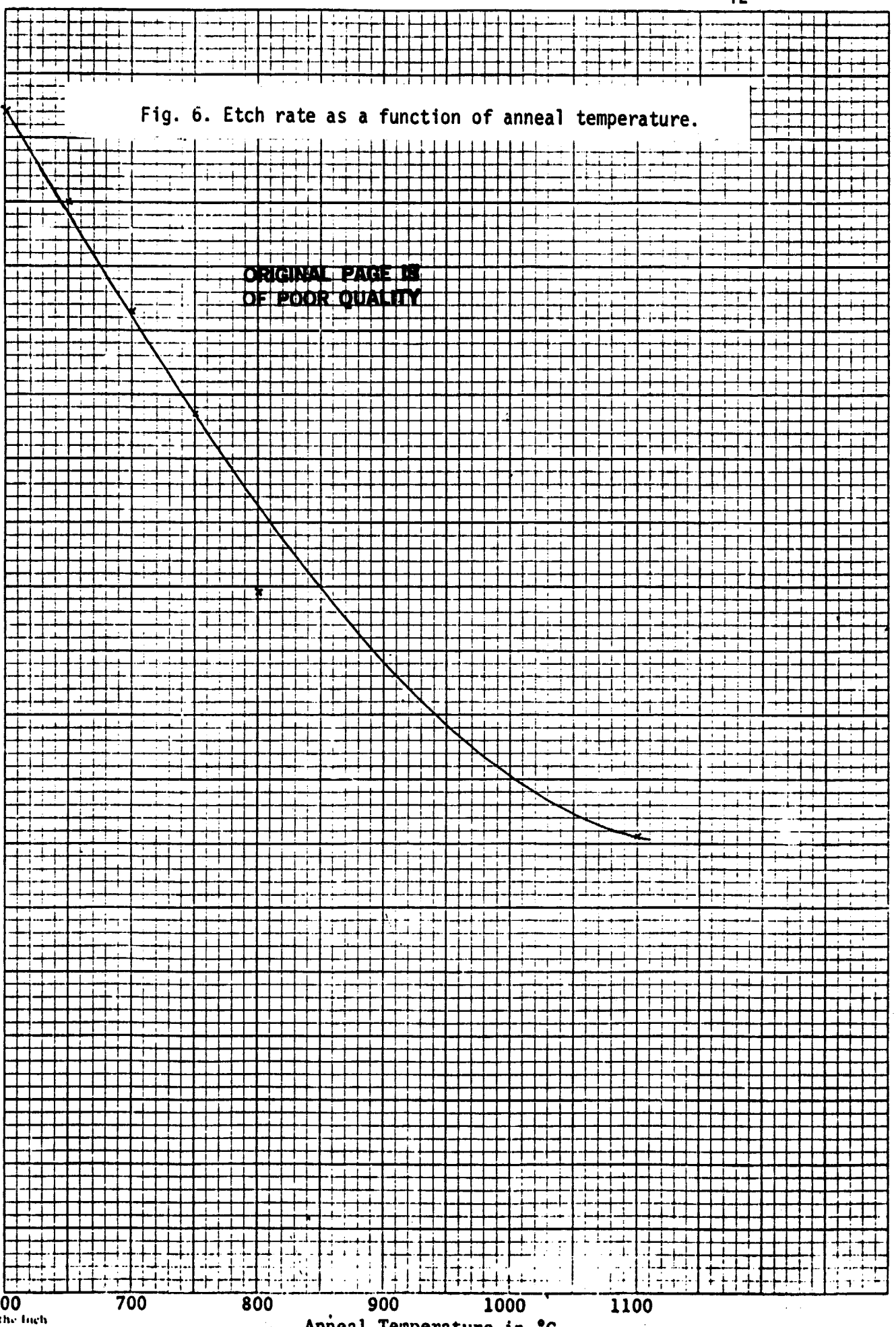


Fig. 5. Dissipation factor as a function of anneal temperature.

12-280

Fig. 6. Etch rate as a function of anneal temperature.



10 Squares to the Inch

voltage was increased slowly. When breakdown occurred, a current pulse would exist in the capacitor. This caused the aluminum metalization at the point of breakdown to melt and evaporate. The result was that the breakdown was self-healing. The power supply voltage could be increased further until the next breakdown point occurred. Several such breakdowns were observed for each of the capacitors tested. Those voltages are given in Table I.

The reason why breakdown occurs at several voltages lower than the theoretical maximum voltage (theoretical maximum field strength multiplied by the oxide thickness) is that imperfections in the electrodes led to a tunnel emission of electrons into the oxide. This process is basically the Fowler-Nordheim injection process and it leads to localized filamentary heating. Because, for the case of thin electrodes, this breakdown can be self-healing, it should be possible to condition the electrodes by burning out weak spots.

1.2.3 Electrode Materials

Electrode materials other than aluminum were investigated in an attempt to avoid some problems which were associated with the oxide-aluminum interaction at the high temperatures which were desired for annealing purposes. Silicon seemed to be a potentially good material from several standpoints. It was fairly easy to deposit by decomposing silane at 450°C using diborane as a catalyst. It has no adverse reaction with silicon dioxide and is stable at high temperatures. One problem of a serious nature does exist, however. That is related to the

Capacitor	Breakdown Voltage Lowest	Highest
A1-10A-3		680
-5	75	500
-6	212	665
A1-11A-5	90	698
-7	168	690
A1-12N-1	180	625
-3	130	630
A1-14AB-1	180	625
-5	135	630
A1-15AB-1	100	625
-7	430	619

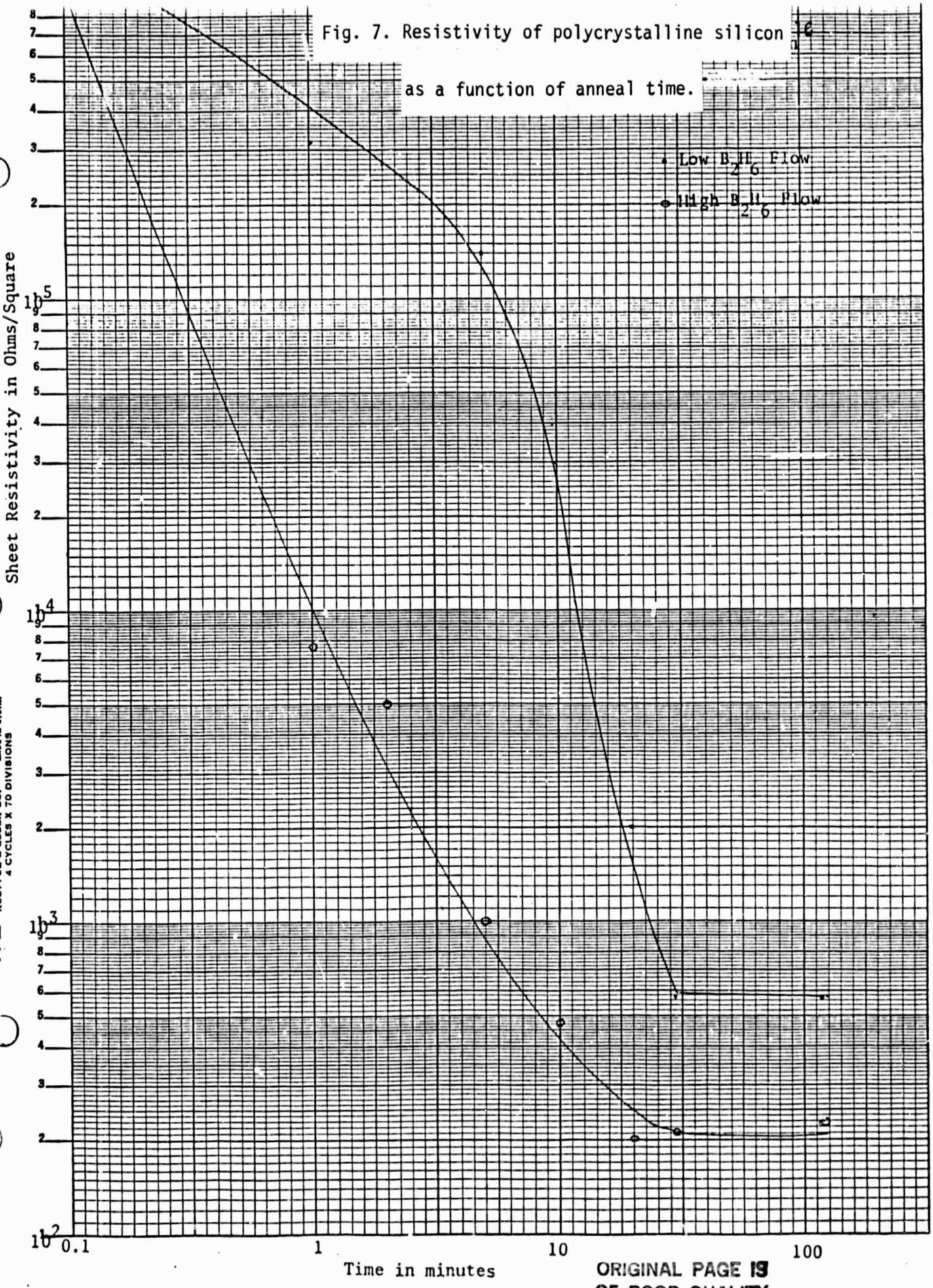
Table I. Capacitor Breakdown Voltages.

dissipation factor increase when capacitors are constructed with such a high resistivity material. The resistivity of the pyrolytically deposited silicon depended on the amount of boron trapped in the silicon during growth as well as the temperature and time at which the silicon was annealed. Figure 7 is a plot of this resistivity variation with annealing time. The lower limit of 200 ohms per square was mainly due to the low diborane concentration which was available. This effectively limited the usefulness of silicon electrodes in this research.

It was thought that perhaps chromium electrodes might be better than aluminum in the anneal temperature range because of the much higher melting point of chromium. Unfortunately, chromium reacts with the oxide at high temperature and seems to disappear into the oxide after only a few minutes at high temperatures. This problem might be overcome by using a thicker deposit. This was not possible during this work because of the difficulty of evaporation of chromium from a resistive heating evaporation boat.

Other electrode materials were also used in an attempt to compare the ease of deposition, annealing characteristics etc. of various materials. An attempt was made to deposit both copper and nickel from electroless solutions. Although this is quite easy when depositing on a conductor, it becomes quite difficult when attempting a deposit on an insulator such as silicon dioxide. No success was ever achieved with the nickel deposit attempts, but some success was noted with the electroless copper deposition. The copper layers were rather thin and non-uniform and no further experiments were conducted.

Fig. 7. Resistivity of polycrystalline silicon as a function of anneal time.



Silver was deposited from an electroless solution of silver nitrate. Although the rate of plating of the oxide was fairly good, the adhesion and uniformity were quite poor. No other electroless solutions were tried.

Gold was evaporated onto the wafers in the hope that it would react less with the oxide during anneal cycles. The stresses in the gold-oxide interface were substantial however, and peeling of the gold occurred when a layer of oxide was deposited on the gold.

It was generally concluded that aluminum seemed to be the best choice for an electrode material when the first attempts at multiple layer capacitors were started.

1.3 MULTIPLE LAYER CAPACITORS

1.3.1 Basic Construction

There are two fundamental problems which must be confronted when multiple layer devices are attempted. One of those problems is that of the interconnection scheme to be used. The other is related to the compatibility of adjacent layers with respect to temperature coefficient of expansion and stresses.

The interconnection difficulties are not as great when only a few layers are used as they are when tens of layers are attempted. One of the possibilities considered was a scheme to vary the doping in the oxide on alternate layers. By using varying amounts of boron doping in the oxide, the etch rate could be controlled over more than an order of magnitude. It was hoped that this would enable selective etching and the ability to interconnect all of the alternate layers. Boron doped

oxides were grown by the addition of diborane - B_2H_6 to the gas phase reaction. Because of the insufficient concentration of diborane available, it was not possible to dope the oxide to a great enough extent to obtain the desired change in etch rate. Only about a two to one reduction in etch rate was obtainable.

When the first attempt at multiple layer capacitors was made, a simple mask geometry was used with interconnection tabs being alternately shifted from one side of the wafer to the other. The first capacitor in the multiple layer structure was tested and there were no shorts between the first (Al-1) and the second (Al-2) aluminum layers. At this point, a second oxide layer was deposited and a third (Al-3) aluminum layer was evaporated. The capacitors were again tested. There were no shorts between Al-2 and Al-3 but all of the capacitors formed by Al-1 and Al-2 were now shorted. The next layer of oxide was deposited and Al-4 was evaporated. The test results showed that all of the capacitors formed by Al-2 and Al-3 were shorted with the Al-3 to Al-4 capacitors being satisfactory. The pattern became quite clear at this point. Apparently, when each successive layer of oxide was grown, the stresses introduced caused previously grown layers to crack and form shorts.

It was speculated that perhaps the silicon substrate might be playing a role in this problem. The same multi-layer capacitor was constructed on a glass substrate which was in fact a high resolution photographic plate. The results were exactly the same as for the silicon substrate - each successive layer created shorts in the previously grown layers.

Because of the different stresses in the oxide which are created when the oxide is doped, it was decided to attempt multiple layer devices using boron doped oxide. The results were worse than before. There were a number of shorts between Al-1 and Al-21 when the first layer was deposited. When the next oxide layer and Al-3 were deposited, again all of the Al-1 to Al-2 capacitors were shorted and in addition some of the Al-2 to Al-3 capacitors were shorted. When the third oxide layer was grown, the entire oxide cracked. The use of boron doped oxides apparently was only increasing the thermal stress problems.

In an effort to better characterize the multi-layer problems, a series of experiments was begun using different procedures for the formation of the multi-layer capacitors. The geometry of the mask used to form the capacitors was changed to that shown in Figure 8. The first experiments were an attempt to determine if silicon as an electrode material would help reduce the stresses between the oxide and the metal electrode. The metal electrode was retained in order to keep the dissipation factor low. The stacking sequence was: Al - SiO_2 - Si - Al etc. After growing the third layer of silicon, cracks began to develop in the layers. Figure 9 shows the resulting wafer.

Next, the above experiment was repeated this time using silicon on both sides of the oxide. The stacking sequence was: Si - SiO_2 - Al -Si - SiO_2 - Si - Al etc. After the third layer, it appeared that the center region began to crack but that the electrode region was not cracked. It seemed then that the aluminum added strength to the structure.

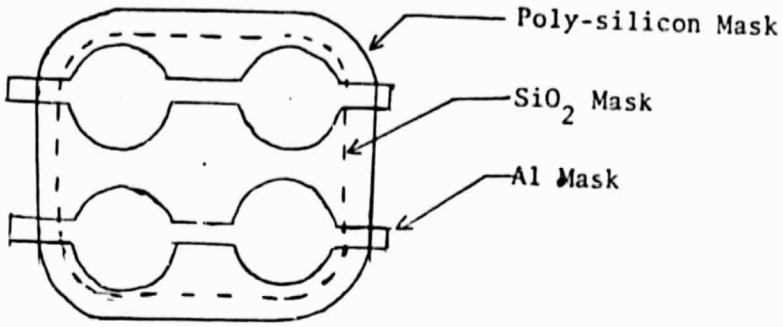


Fig. 8 Modified mask geometry for multi-layer capacitors.

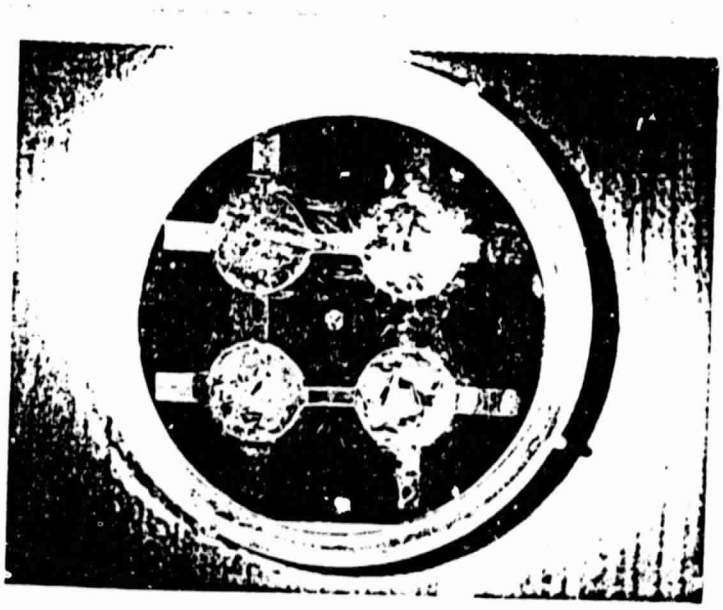


Fig. 9. An Al - SiO_2 - Si - Al etc. structure.

A vertification of the conclusion about aluminum adding strength to the system was made by repeating the above mentioned structure without the aluminum present. This time the entire structure developed cracks, even in the electrode regions, thus confirming the idea that the aluminum adds strength.

Additional work using silicon as a buffer was done by increasing the thickness of the silicon using the Al - Si - SiO_2 - Si - Al etc. structure. When cooled to room temperature, cracks developed which seemed to propagate from the edge.

Most of the evidence up to this point indicated that it was the very thick oxide and/or Si - SiO_2 regions which cracked first. In order to determine the maximum thickness of oxide which could be tolerated in any region, oxide was grown on a wafer until cracks began to occur. Our test wafers showed that cracks appeared after about 2 microns of growth.

Quite a number of factors affect the tendency of the layers to crack. For example, if an oxide layer became contaminated after growth, the adhesion of the aluminum was quite poor. The photograph in Figure 10 shows such a wafer.

To eliminate the problem of thick oxide build-up, the mask configuration was changed to make the oxide mask cover only the electrode area as shown in Figure 11. Capacitors were constructed which consisted simply of alternating layers of aluminum and silicon dioxide. Upon deposition of the fourth layer of oxide, a loss of adhesion occurred between the third layer of oxide and the fourth aluminum layer. The oxides were cracked between layers and the electrodes were shorted.

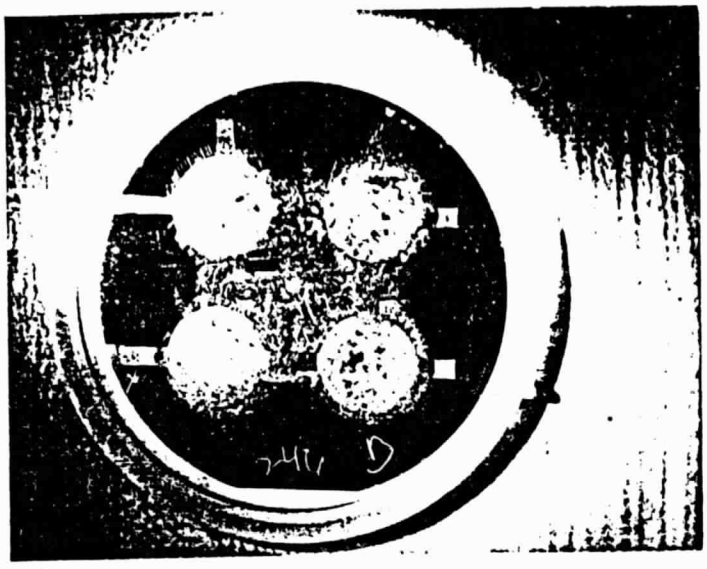


Fig. 10. Loss of adhesion due to contaminated oxide.

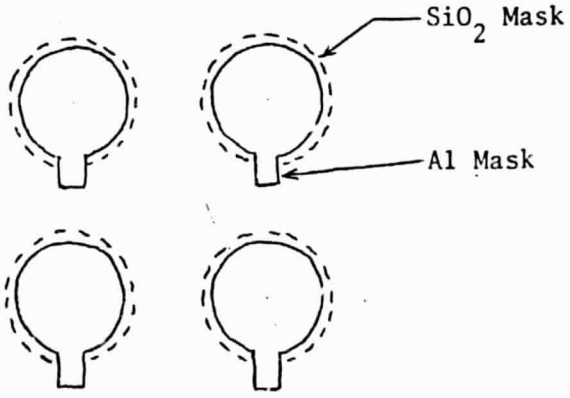


Fig. 11. New mask geometry to eliminate the thick oxide regions.

There were two distinct problems which occurred. One was cracks in the oxide. This led to shorts which couldn't be blown out. The second problem was loss of adhesion between layers. As the previously run experiments showed, elimination of one problem often led to the creation of the other. In some cases, both problems were present at the same time. The adhesion problem was the one that was examined in detail first.

An experimental structure consisting of alternating layers of oxide and a thick aluminum deposition was made without using any masking. This arrangement resulted in ten layers being achieved with no loss of adhesion. However the oxide did develop cracks and all the layers were shorted. The same test was repeated using a much thinner aluminum evaporation. The structure was carried through to ten layers, but some loss of adhesion occurred on the eighth layer wherever foreign particles had fallen on the surface. Here again, the oxides were cracked and the electrodes were shorted to each other.

Thus it appeared that the loss of adhesion problem could be overcome with the oxide-aluminum system through proper processing procedures. The cracking problem was more difficult to solve. It was presumed that the stresses introduced in the oxide during the evaporation of aluminum led to the cracks upon heating. This thought led to the experiment referred to as the hot deposition approach.

Previously, the aluminum was not evaporated until the oxide was cool. This meant that when the next oxide layer was added, the thermal

coefficient of expansion of the oxide being different from the aluminum would lead to stresses and oxide cracks. To overcome this, a capacitor was constructed in which the aluminum was evaporated while the oxide was still hot. A three layer device was made which resulted in no cracks or shorts. This was a clear demonstration that the cracking problem was due to the stresses developed in the oxide. After about three days, however, there was a loss of adhesion on parts of the electrodes of this capacitor.

1.3.2 Phosphosilicate Glass

The evidence associated with the numerous experiments conducted up to this point now led to the following conclusions. Firstly, the use of an aluminum-silicon dioxide system seemed to be the best choice from the overall point of view. Secondly, the loss of adhesion problem could be controlled through proper processing. Thirdly, the cracking problem was definitely due to stresses in the oxide at the oxide-aluminum interface. The clear choice at this point was to find a way to reduce the stresses in the oxide.

The available literature gave some help in this area. Stress measurements on phosphorus doped oxide indicated that the formation of a phosphosilicate glass (PSG) significantly reduced stress problems and improved yields associated with such things as integrated circuits. Thus it was decided to add a phosphorus doping capability to our pyrolytic oxide reactor.

Because of the quantity of phosphorus required in the oxide, extreme care had to be taken in the installation of the system to insure

the safety of personnel. Phosphine was used as the phosphorus source and it is extremely toxic. The entire system, including the tank of phosphine gas mixture, was kept entirely within the confines of the fume hood in which the reactor was installed.

The concentration of P_2O_5 in the oxide was predicted analytically from the gas flow information. It was measured using infrared spectroscopy. The agreement between the predicted value and the measured value was excellent. Shown in Figure 12 is an IR transmission curve showing the absorption dip due to the phosphorus-oxygen bond. Shown in Figure 13 is a plot of the measured and calculated values of PSG composition as functions of the flow rate of the phosphine mixture.

Some shorting of capacitor layers almost always occurred when the number of layers wassufficiently large such that the surface irregularities created cracks in the PSG. Although most such shorts could be blown out by a discharge pulse from a large capacitor, it was nevertheless desirable to minimize the occurrence of such shorts. To that end we studied the problem of delineating small micro-cracks in order to determine which process parameters to vary in order to reduce crack formation.

Normally for PSG layers over aluminum all that is required is to place the samples in an etch that will easily attack the underlying aluminum. Such things as hot HCl are commonly used. It is not as easy however to show up the cracks over silicon. This is of some importance in this work since we are currently using a silicon substrate on which the alternating layers of aluminum and PSG are deposited. To this end

Fig. 12

I.R.Absorption spectrum of PSG using plain Si wafer as a reference on Perkin Elmer Model 180 Spectrophotometer

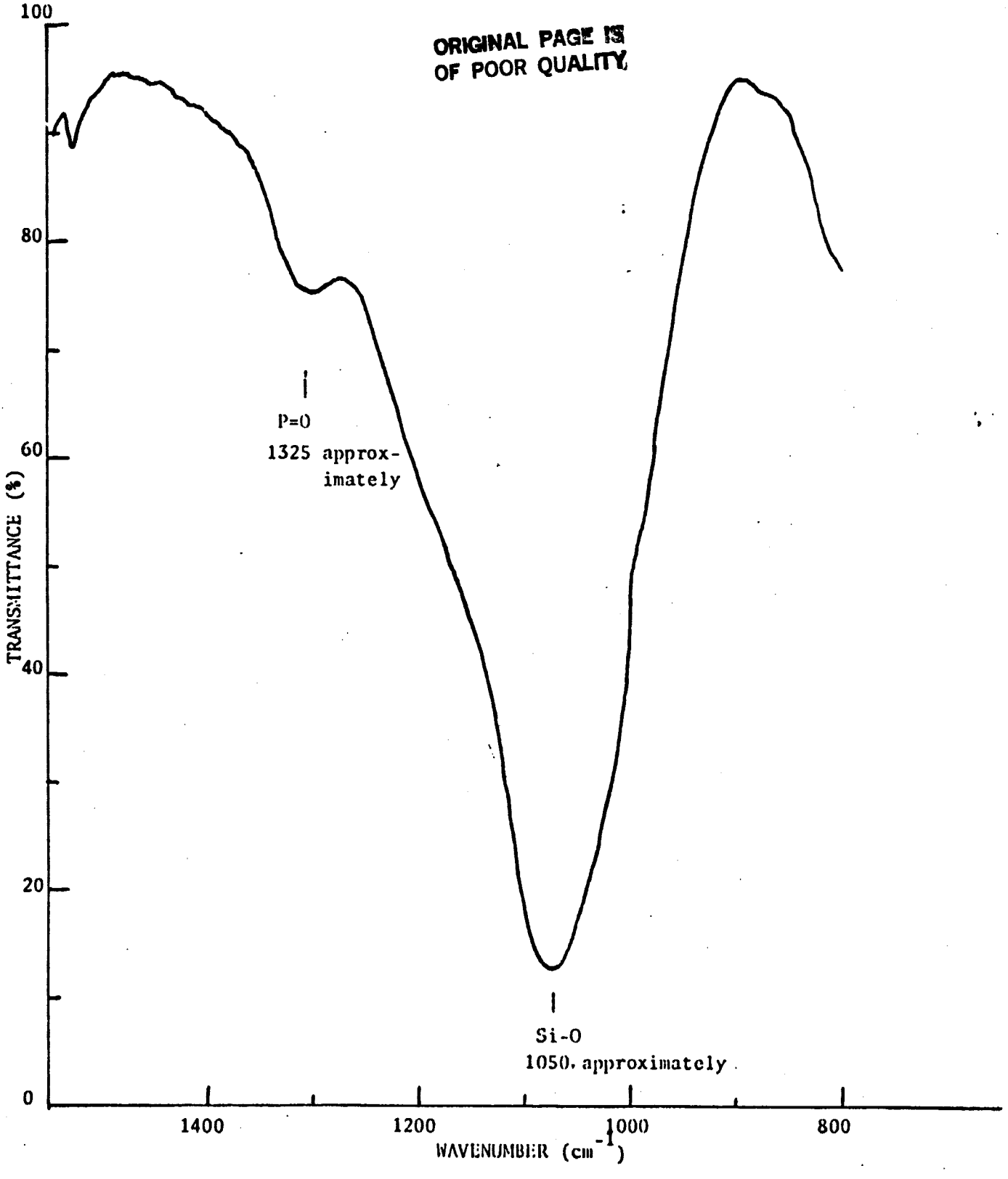
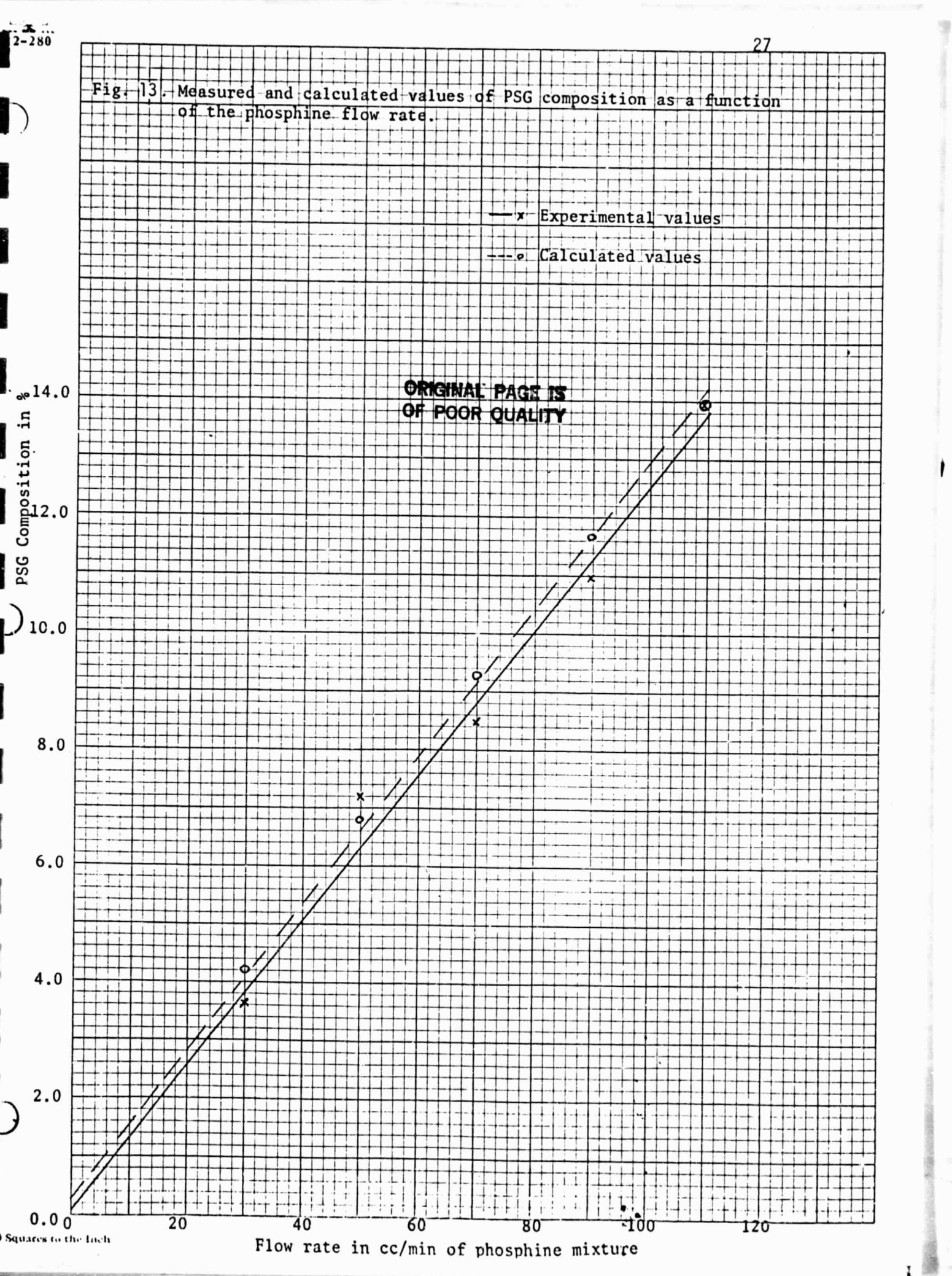


Fig. 13. Measured and calculated values of PSG composition as a function of the phosphine flow rate.



we developed a new etch which seems to work quite well for the delineation of cracks and pin holes in PSG deposited on silicon. The etch is fast acting and easy to use.

In order to test the etch, a 1 μm layer of PSG was deposited from a SiH_4, O_2 and PH_3 mixture at a temperature of 400 °C onto 2" polished silicon wafers. The coated wafers were then removed from the reactor and cooled rather rapidly so as to induce cracks in the PSG.

The wafers were then put into the etch solution which consisted of a mixture of H_2O, HF and H_3PO_4 in the ratio 60:3:1. The HF and H_3PO_4 were 48% and 85% respectively as received in the bottles. The ratios given were not extremely critical to the success of the etch.

No cracks were visible either to the unaided eye or through a microscope prior to placing the wafers in the etch. When the wafers were placed in the etch, the larger cracks almost immediately became visible even without the use of a microscope. Only about 30 s in the etch is necessary to delineate most cracks. The etch works well with a wide range of PSG concentrations but does not seem to delineate pin holes in undoped SiO_2.

This was one of the many evaluation tools available to use for the detection of imperfections in process procedures. It was not as useful when the surface became rough after the deposition of a large number of layers. In such cases, the SEM was a better anlaysis tool.

There is some interaction between aluminum and un-doped silicon dioxide resulting in the formation of aluminum oxide and silicon. This is however rather slow and completely negligible at temperatures below

approximately 450°C. With phosphosiliate glass the situation is considerably different. The presence of phosphorus pentoxide leads to the formation of phosphoric acid if any moisture is present. There is water formation during the growth of the PSG and as a result part of this is trapped in the oxide. The resultant phosphoric acid will readily attack aluminum even at a few hundred degrees of temperature.

Because such an attack on the aluminum could create dissipation factor problems, we decided to set up some basic experiments to determine the degree to which such a reaction would affect our thin aluminum layers. The basic approach used was to deposit thin film resistors of aluminum over PSG and to monitor the resistance as a function of time and temperature. As the reaction between the aluminum and PSG proceeded, it would reduce the thickness of the aluminum thereby increasing the resistance.

Because the resistors were rather low in value, it would have been best if a Kelvin double bridge were available with which to make the measurements. Since one was not conveniently available the measurements were made by a rather conventional voltmeter-ammeter method.

Two different tests were run, one at room temperature and the other at 250°C. The results of the room temperature test showed an increase of approximately 7% in resistance over a 100 hour period. The data were rather scattered and the precision of the measurement was such that some of the statisical significance of this was lost. For the 250°C test the results were quite clear. The resistor increased an average of 24% in 115 hours. This translates into an estimated rate of attack of the

aluminum of 3.9A/hr. That is not negligible since the aluminum layers are being attacked on both sides resulting in the loss of aluminum at the rate of 7.8A/hr.

The standard fabrication procedure for multilayer capacitors was to keep the capacitors at an elevated temperature of 200-250 °C in between the times that the layers were being deposited. Since that occurred over a period of up to two or three weeks if delays were encountered, it created an appreciable loss of aluminum. Thus this is a factor which had to be considered in the processing. Clearly the total time span of multiple layer deposition must be kept as short as possible or else the capacitors must be returned to room temperature in between layers. It was necessary to follow the latter course of action for the capacitors which had greater than 20 layers.

1.3.3 Ten Layer Capacitors

There were two different ten layer capacitors sets constructed using 7% PSG. One of them used a hot deposition technique for the aluminum, the other used a cold deposition. Each set was tested every four layers and shorts due to oxide pin holes were blown out. Neither set initially showed either cracks or loss of adhesion. After ten days, one of the capacitors in the set which had been fabricated with the hot deposition method peeled due to loss of adhesion. This can be seen as the small black speck on one of the capacitors in Figure 14. Capacitance as a function of frequency is shown in Figure 15.

The 10 layer capacitors have been studied further by scanning electron microscopy to determine the relative uniformity of the layers. The SEM pictures are shown in Fig. 16 and illustrate the appearance

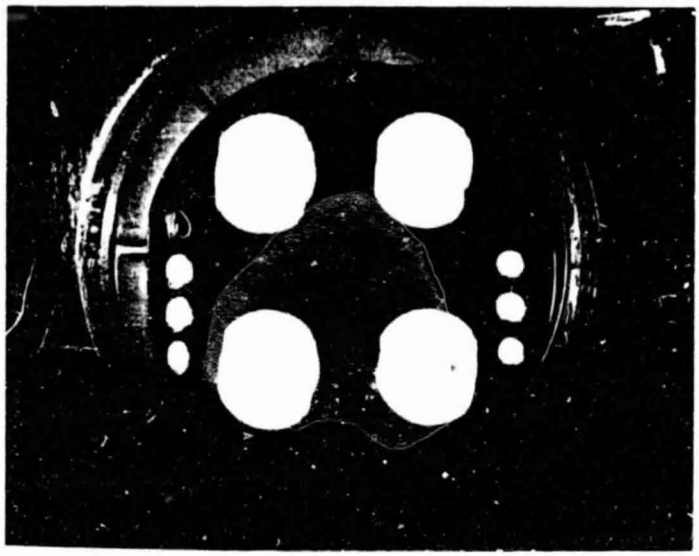


Fig. 14. Ten layer PSG capacitor by hot deposition method.

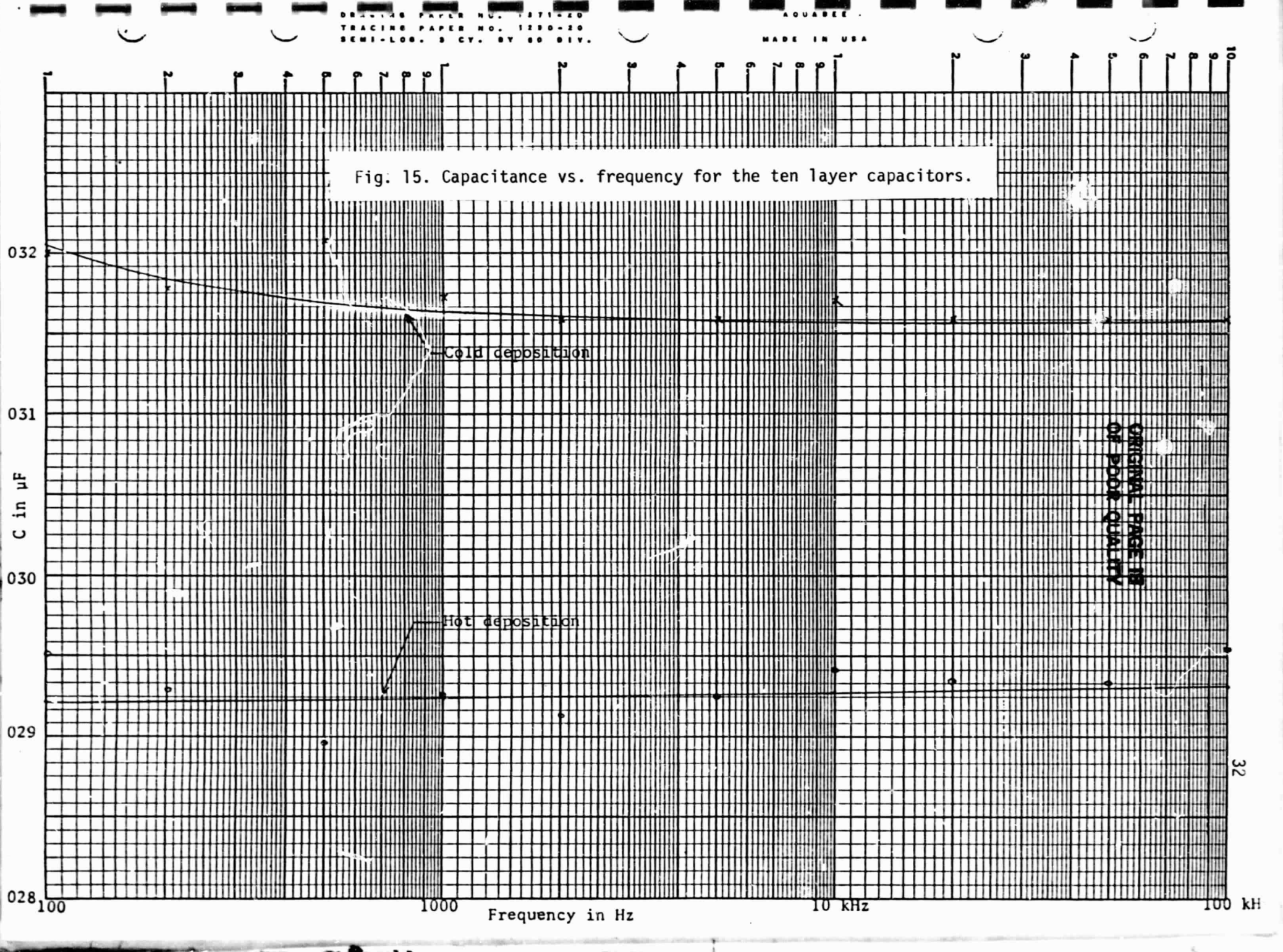


Fig. 15. Capacitance vs. frequency for the ten layer capacitors.

under increasing mangification. Because of a calibration error on the SEM screen, the size markers, visible on the left side of each picture, are in error. The relative magnification can be judged easily, however, because the oxide layers, which are the dark bands, are within 5% of 1μm in thickness. This has been determined from previous measurements under the same growth conditions.

The pictures show several things of interest. In the photos it is clear that the surface does contain an appreciable number of irregularities. Part of these are probably due to dust etc. picked up while preparing the sample for insertion into the scanning electron microscope. Part of these irregularities are actually in the layers as can be seen rather clearly in Figure 16c. This is due in part to very small particulate matter being trapped in the oxide layers during growth. The size of these particles is quite small, approximately 1 to 2 and hence quite difficult to control.

As the layers grow in number, the small perturbations which are introduced into the first layers are magnified by each additional layer. This will ultimately create serious difficulties in the form of shorted layers. This effect is shown rather clearly in Fig. 16c.

The edges of some of the aluminum layers were studied under the SEM. It is significant to note that there was relatively little problem due to such edge effects. The oxide layers made the transition smoothly. Thus the particular scheme which was chosen for alternating metal layers by shifting the metal evaporation mask seemed to be a quite satisfactory method.

a.

b

c

Fig. 16. SEM photos of an early 10 layer capacitor.

There seemed to be quite a bit of variation in processing control as far as the uniformity of the particulate contaminant problem was concerned. Shown in Fig. 17 is a cross section of a 10 layer capacitor made about three months after the one shown previously. Note that it is quite a bit more irregular. It is concluded from this that minor variations in process steps and reactor cleanliness have an appreciable effect on the smoothness of the layers.

1.3.4 Twenty Layer Capacitors

In the next phase of our efforts, we constructed 20 layer capacitors. In Figs. 18 and 19 are shown plots of the capacitance and dissipation factors as functions of frequency. The measurements were taken on a model 250 DE impedance bridge made by Electro Scientific Industries. As can be seen, the capacitance is quite constant with frequency. The increase in dissipation factor with frequency indicates a series resistance in the capacitor, rather than a shunt leakage. This series resistance is probably due to the rather thin metal layers which are being used and the attack of that metal by the PSG. This can potentially be corrected by using a thicker metallization.

The DC leakage current was measured for each of the three capacitors at a test voltage of 10 VDC. The results are given in Table II along with the capacitance values and dissipation factors at 1 kHz. These values are quite small considering that the capacitors have an area of approximately 1 cm^2 and the leakage is the sum of that due to 20 different layers.

Shown in Fig. 20 are scanning electron microscope photographs of the cross section of one of the 5 capacitors made during the twenty

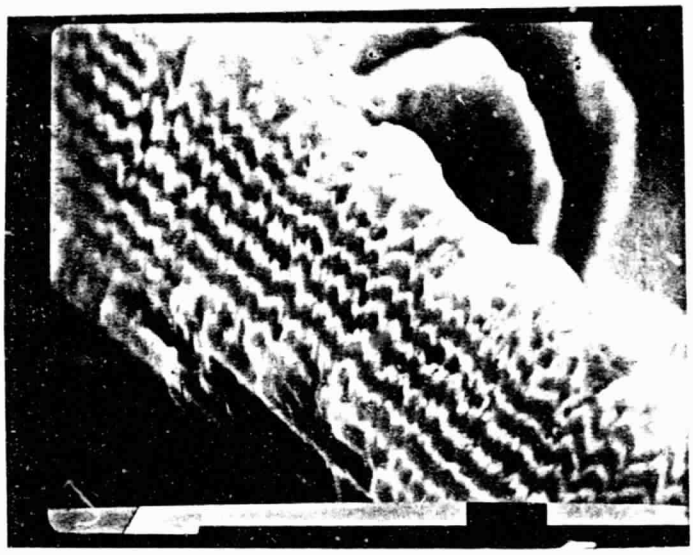


Fig. 17. SEM photograph of a later 10 layer capacitor.

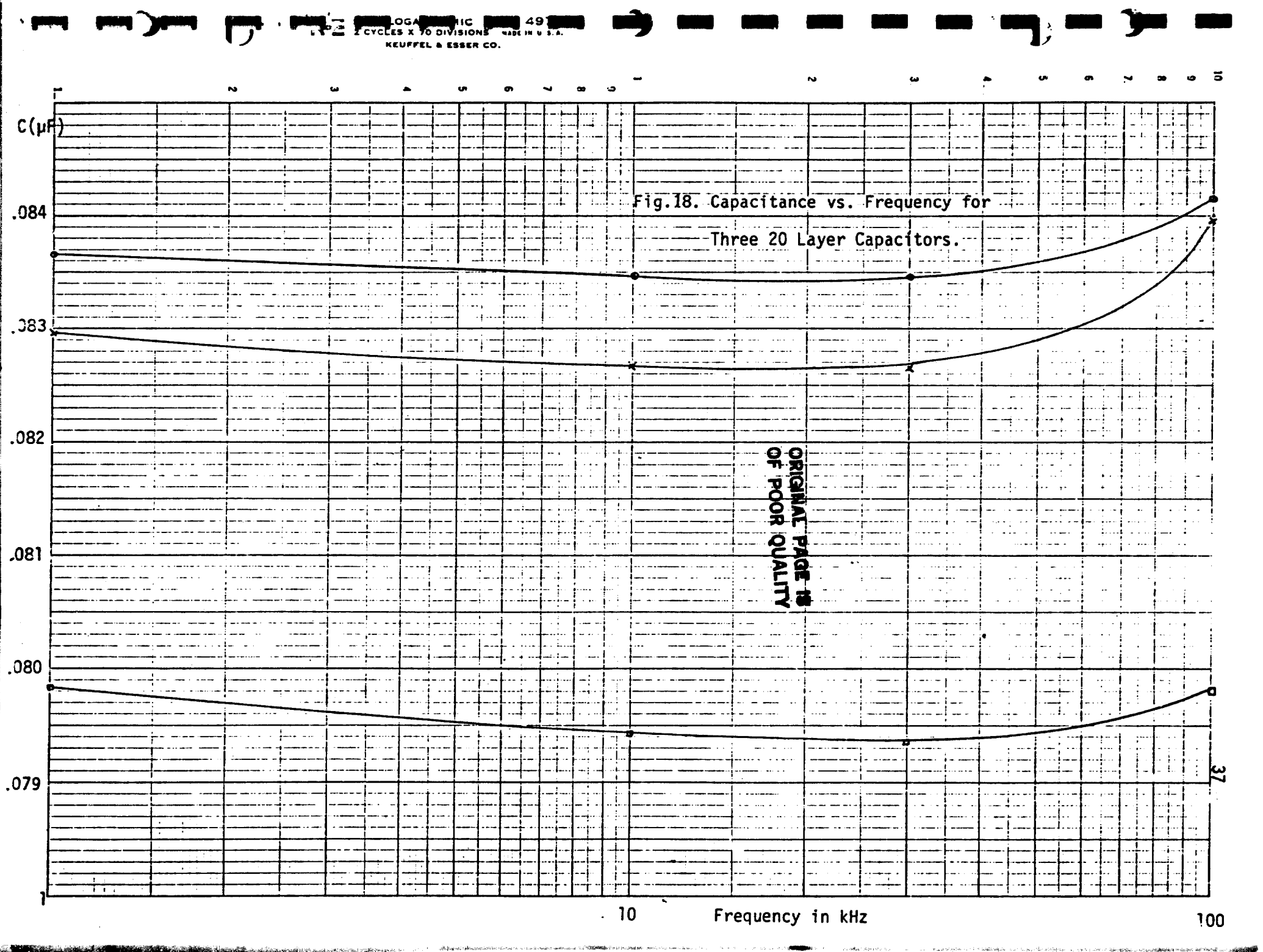


Fig.18. Capacitance vs. Frequency for Three 20 Layer Capacitors.

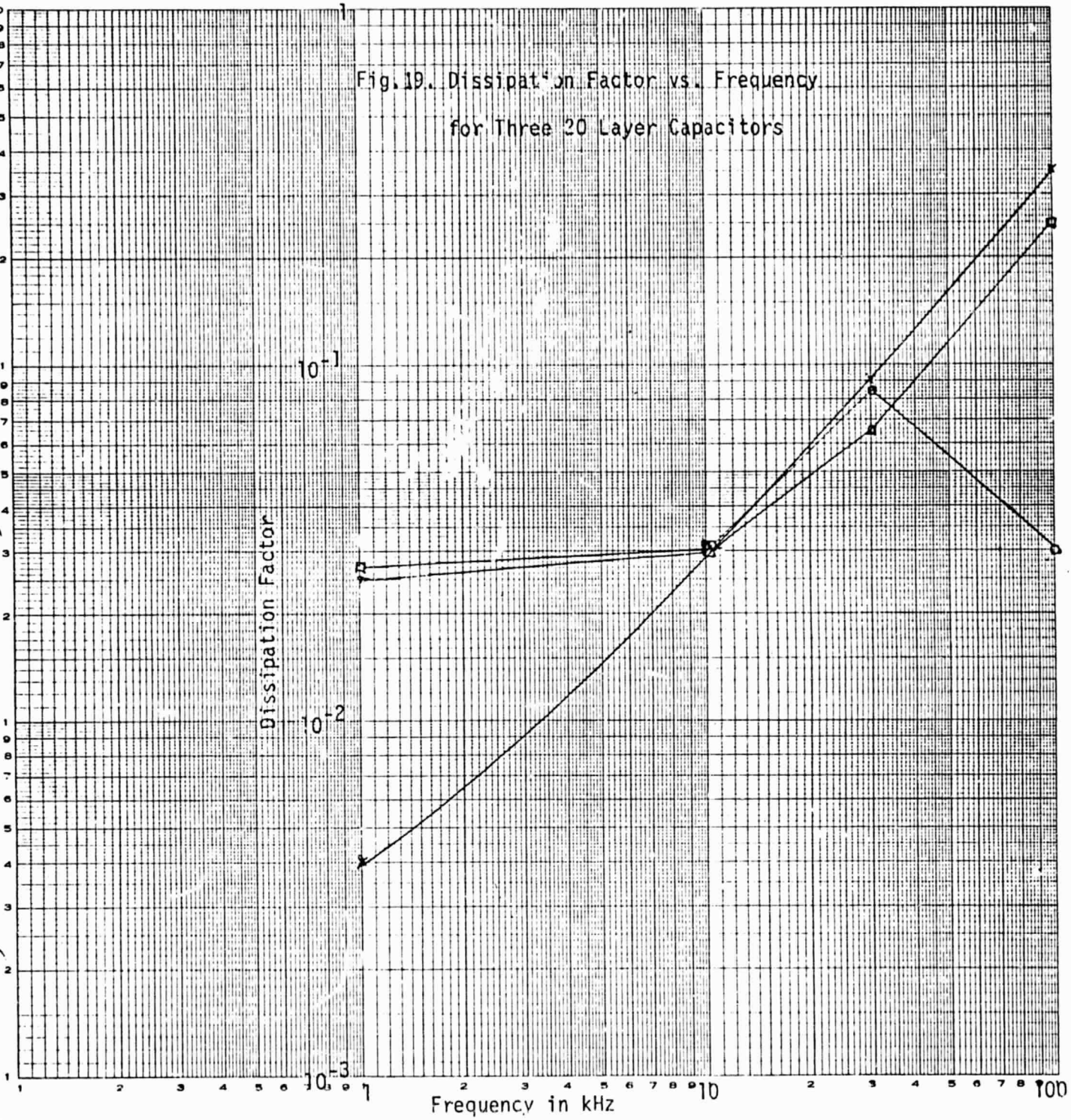


Fig. 19. Dissipation Factor vs. Frequency for Three 20 Layer Capacitors

Cap. No.	C	D	Leakage @ 10 VDC
	μF		ηA
1	.082975	0.004	0.08
2	.079830	0.027	78.0
3	.083655	0.0251	220.0

Table II. Capacitance, dissipation factor and leakage currents of the three 20 layer capacitors.

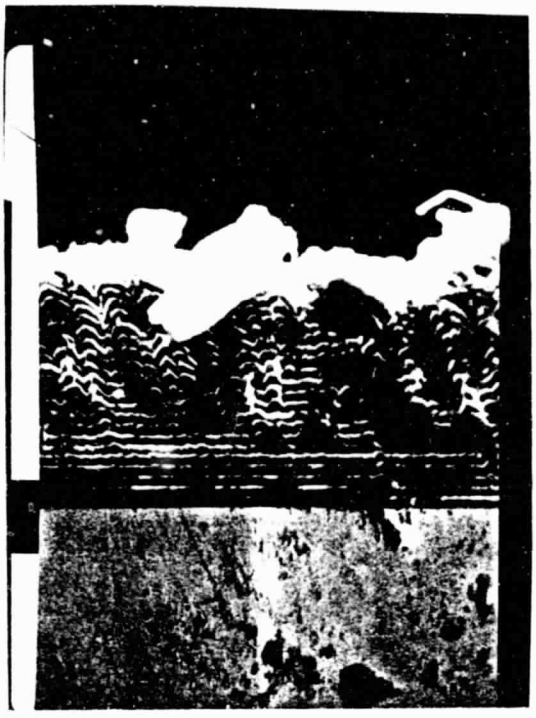
layer attempts. Two of the capacitors developed shorts, the other 3 were good. These photographs show very clearly and unfortunately that the problems associated with surface and layer irregularities can become rather bad when a large number of layers is grown. In fact, considering how bad the upper layers appear, it is amazing that any of the capacitors worked. And yet, 60% were not shorted. This is attributable no doubt to the ability of the phosphosilicate glass dielectric to conform to the surface irregularities without cracking or developing pin holes. These capacitors were made using a silicon dioxide doped with 7% P_2O_5.

A careful study of the SEM photographs does reveal an interesting point, however. Note that the gross irregularities seem mainly to begin at around the 6th layer and that up until that point there was much les irregularity. This suggests that perhaps that layer was accidently contaminated or that something occurred during the processing which was not noticed by the operator.

1.3.5 Stress Measurements

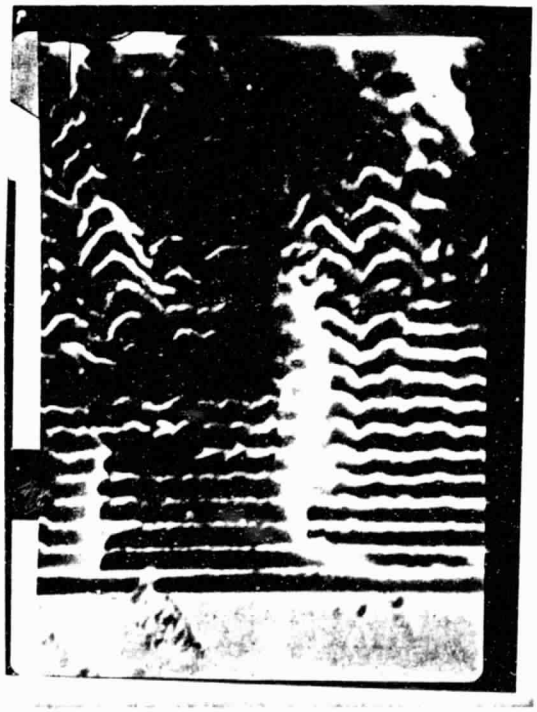
There were a number of problems present in the construction of the 20 layer capacitors. Those problems were mainly in the area of surface roughness and oxide stresses. Because the surface layers were quite irregular, on the order of 3 to 4 μm, it was clear that this would be a major limitation in extending the number of layers beyond that point. Consequently an extensive study of the stress problems was conducted.

In the multi-layer capacitor construction which had been done previously, the phosphosilicate glass (PSG) composition was in the



a

b



c

Fig. 20 SEM photos of a 20 layer capacitor.

range of 7 to 10% P_2O_5. No attempt was made at that time to optimize the percent of P_2O_5 with respect to the capacitor construction. In this phase of our work, we attempted to determine some of the parameters which were creating stresses in the oxide, such as P_2O_5 concentration, and to design a better growth procedure so that the stresses could be reduced without compromising the capacitor quality appreciably.

There are several factors which affect the stresses which exist in the deposited PSG. The principal ones are growth rate and temperature, percent of P_2O_5 in the oxide and moisture content of the oxide. We did not perform any studies on the effect of moisture content in the oxide. Kern et al. indicates that some moisture added to the nitrogen during deposition reduces the stress in the deposited oxide. Our work dealt mainly with the stress reduction by the addition of P_2O_5 and partly with stress reduction by the control of the growth rate.

The experimental procedure which would have been ideal for stress determination would have been to hold the wafer perfectly flat during deposition so that the stress after deposition would cause the greatest amount of wafer bending and hence make the stress determination easier to observe. An attempt was made to construct a vacuum chuck to serve this purpose. It did not turn out to be satisfactory because of slight irregularities on the surface which caused the silicon wafers to crack when the vacuum was applied. As a result the oxides were grown in the normal manner with the wafers not held rigidly in place.

The oxide doping was measured by IR absorption spectra and compared to that calculated from gas flow rates. The agreement is good as shown

in Table III. In addition the etch rate of each composition was measured in a buffered HF solution. That data also appears in Table III.

Oxide doping was varied from 2% P_2O_5 up to 10% P_2O_5. For each case the stress was determined by measuring the amount of bending of the substrate before and after oxide growth. The curvature was determined through the use of an optical microscope which has the capability of measuring vertical displacement to within 0.1 mil. Thus by simply changing the substrate position and re-focusing the microscope, it was possible to plot a profile of the wafer curvature as shown in Fig. 21 for one particular case.

From this data, it was possible to compute the stress through the use of the following equation derived by Glang et al.,

$$\sigma = \frac{\delta}{r^2} \frac{E}{3(1-\nu)} \frac{t_s^2}{t_f}$$

where σ = stress (dynes /cm^2)

δ = deflection of the substrate (cm)

ν = poisson's ratio for the substrate

E = Young's modulus of the substrate

r = radius of the substrate (cm)

t_f = oxide thickness (cm)

t_s = substrate thickness (cm)

The data for stress for each doping level are given in Table IV. Shown in Fig. 22 is a plot of the tensile stress as a function of molar percent of P_2O_5 in the oxide. This curve is close to that published by Kern. The main difference is that our growth rate was much lower than that used by Kern. In fact it was one order of magnitude lower, thus considerable differences in stress would normally be expected.

Table III. Percent PSG and PSG etch rate.

% P_2O_5 IR Spectra	% P_2O_5 Gas mole ratio	Etch rate Å/min
0	0	3318
3.38	3.79	3984
7.0	5.32	5072
8.78	7.53	5760
11.08	8.64	4788
11.08	11.36	5703

Measurement of surface profile using Depth of focus method

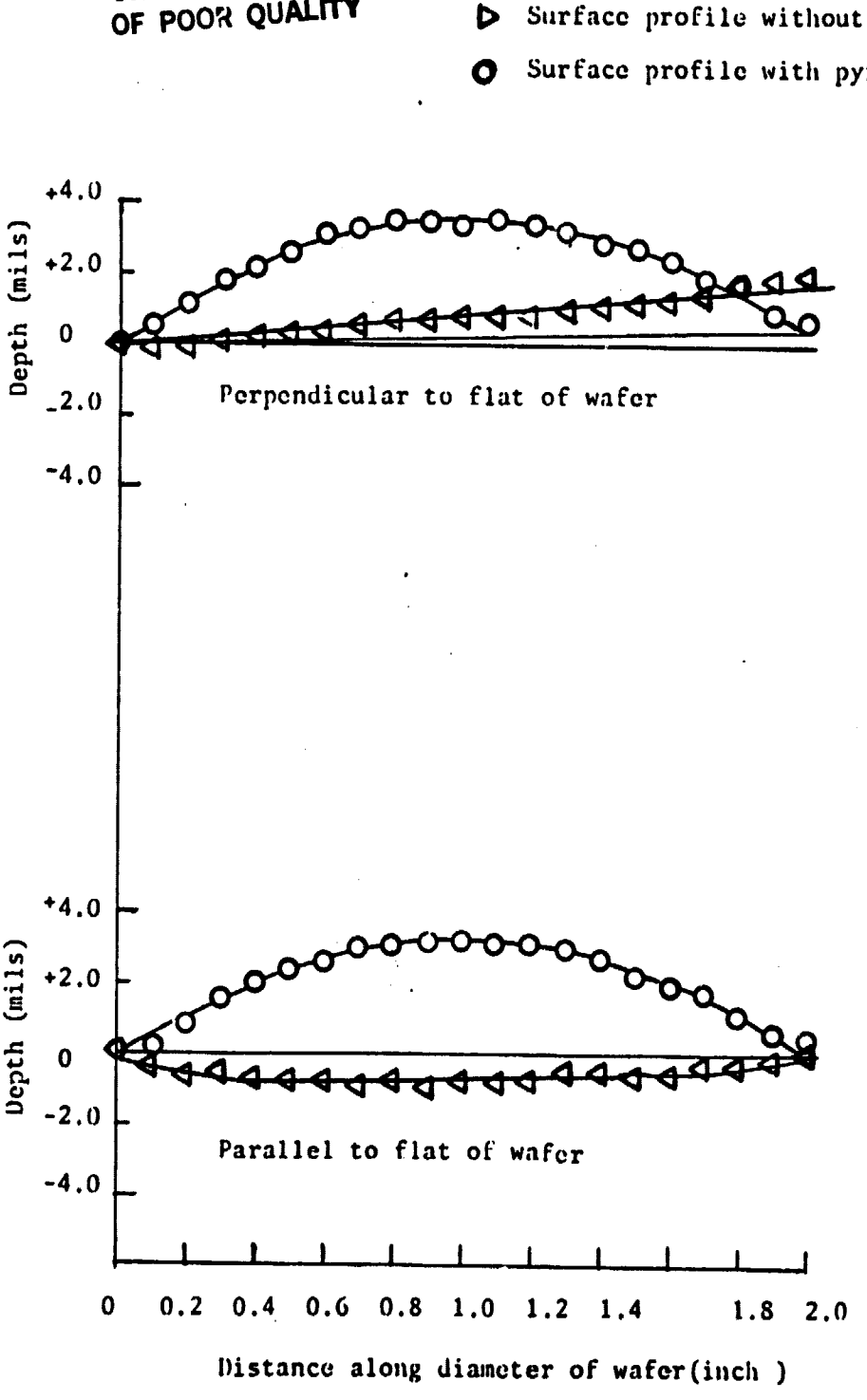
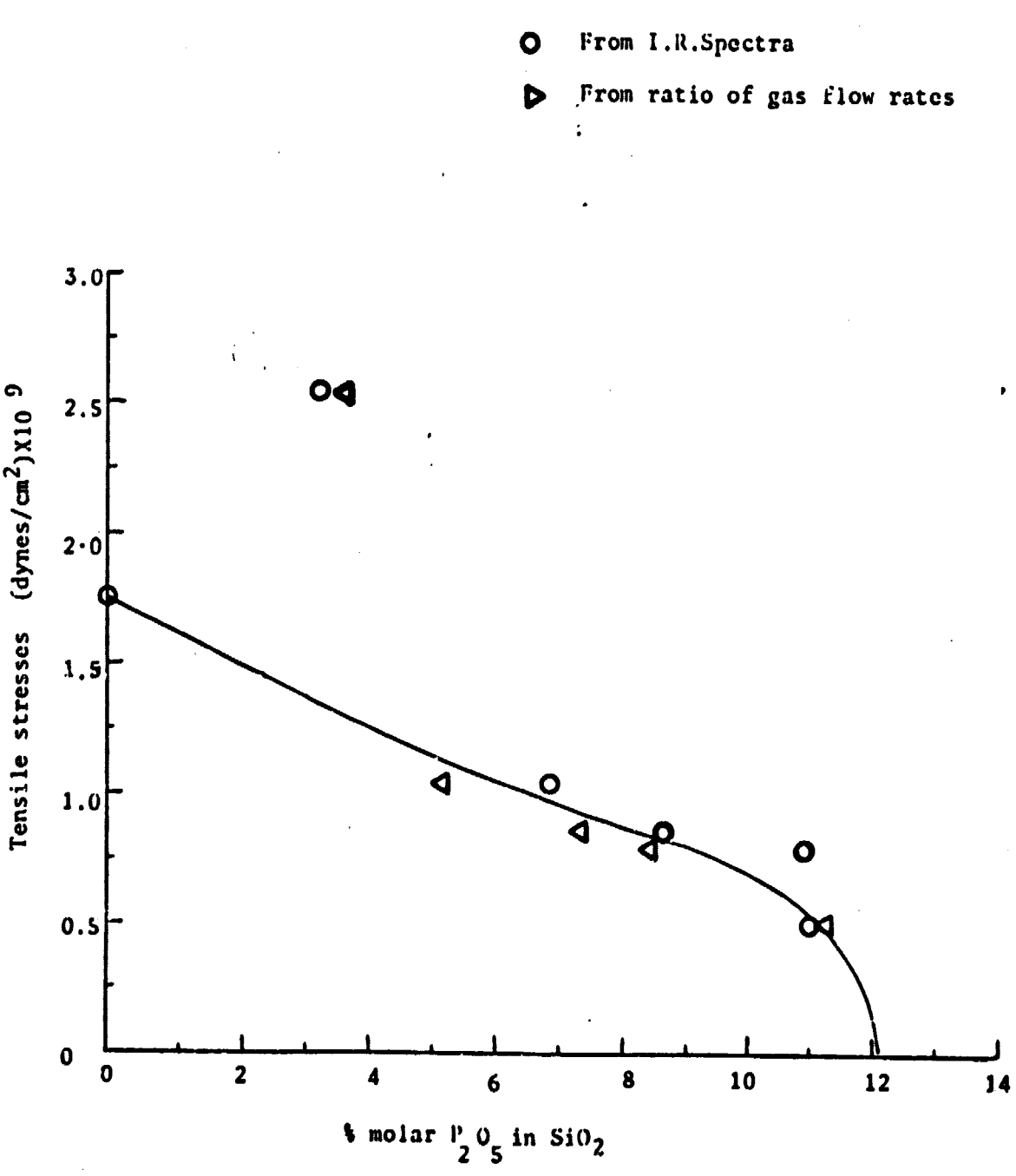


Figure-21

Table IV. Stress as a function of doping level.

Growth rate A/min.	% P_2O_5 IR Spectra	% P_2O_5 Gas mole ratio	Tensile stress dynes/cm^2
720	0	0	1.56×10^9
850	3.38	3.79	2.56×10^9
820	7.0	5.32	1.04×10^9
720	8.78	7.53	0.86×10^9
830	11.08	8.64	0.80×10^9
770	11.08	11.36	0.51×10^9

Fig. 22
Tensile Stresses as a function of %of molar P_2O_5 in SiO_2



One result of our measurements is to note that we must go to very high P_2O_5 levels, perhaps as much as 15%, to reduce the stress to zero. This is an unacceptably high level due to attack of the aluminum by the PSG. Thus a compromise will have to be made between stress and PSG doping level. There are other techniques for controlling stress such as control of the growth rate and moisture level of the incoming gases.

1.3.6 Buffered Oxide Layers

As previously discussed the higher concentrations of P_2O_5 in the oxide reduce the stress and hence the tendency toward cracking and peeling. However the sacrifice which must be made is increased chemical interaction with aluminum. In an attempt to deal with these conflicting requirements, several attempts were made in the construction of a variable doping oxide layer such as shown in Fig. 23. For this structure the oxide layer which is in immediate contact with the aluminum has a reduced concentration of P_2O_5 in order to reduce the attack of the aluminum while most of the oxide layer has a higher concentration of P_2O_5 to reduce the stresses in the main thickness of the oxide.

Three such capacitors were constructed. In each case the oxide growth rate was 1000A/min, the thickness of the main oxide region was 0.9 μm and the two buffer regions of lower doping were each 0.05 m thick. The first attempt was only a 15 layer capacitor in which the main oxide region was doped with an 8% PSG while the buffer regions were completely undoped. A photograph of this capacitor set is shown in Fig. 24. Although it is somewhat difficult to see in the photograph, there

Cross section view of a variable doping oxide capacitor

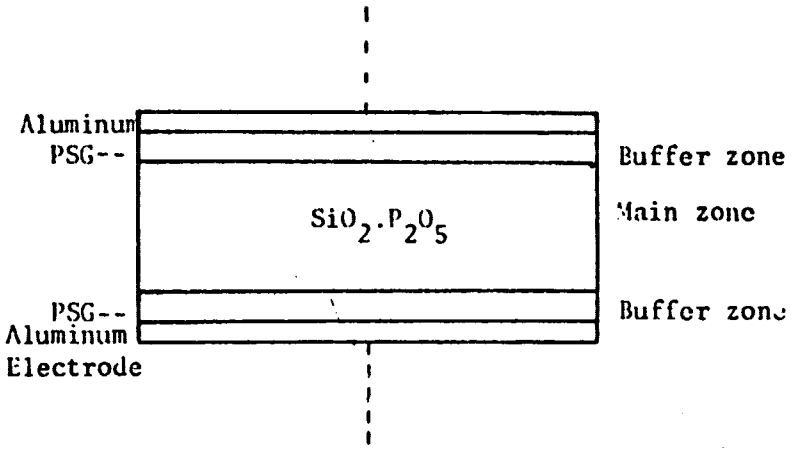


Fig. 23

are quite a number of oxide cracks which can be seen as the dark lines on each of the 5 capacitors.

A second attempt was made by reducing the main oxide layers to 6% and increasing the buffer regions to 4% PSG. There were still an appreciable number of cracks in the oxide on the capacitors. This set was a 20 layer capacitor set. A third set of 20 layer capacitors was made in which the main oxide doping was 8% and the buffer regions were 6%. This still resulted in oxide cracks which are visible in Fig. 25. However, there were fewer and less severe cracks in this case. It thus appeared that it was necessary to go to a rather highly doped buffer layer in order to avoid stress induced oxide cracks.

The capacitance and dissipation factor were measured for the 20 layer capacitors at a frequency of 1 kHz. The data for those capacitors are given in Table V. Although the dissipation factor is rather high, it should be pointed out that this is measured at 200°C. It would certainly be lower at room temperature. Measurements of capacitance and dissipation factor were not made at lower temperatures because both capacitors cracked when they were cooled down. Although we cannot be perfectly certain, it is likely that the dissipation factor at room temperature will be an improvement over the values obtained with the previous 20 layer capacitors.

Our previous 20 layer capacitor suffered from appreciable surface irregularities as was noted in the scanning electron micrographs. To overcome these problems, several processing changes were made. One of the processing changes made was the increase of substrate temperature

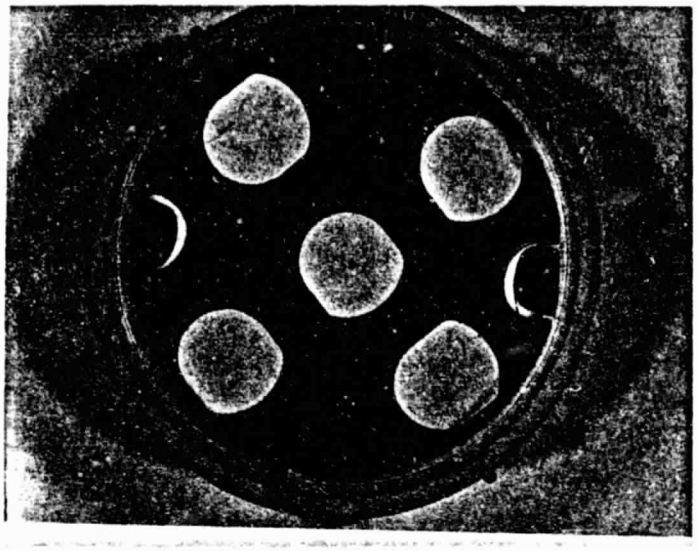


Fig. 24. Photograph of the 8%/0% 15 layer capacitor set.

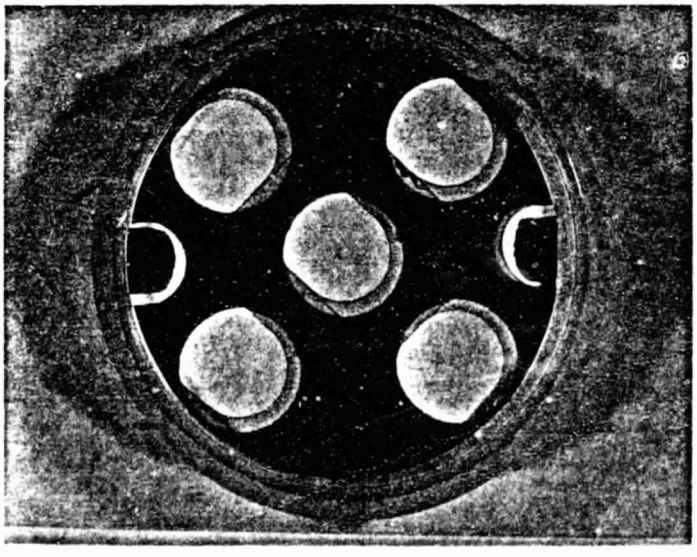


Fig. 25. Photograph of the 8%/6% 20 layer capacitor set.

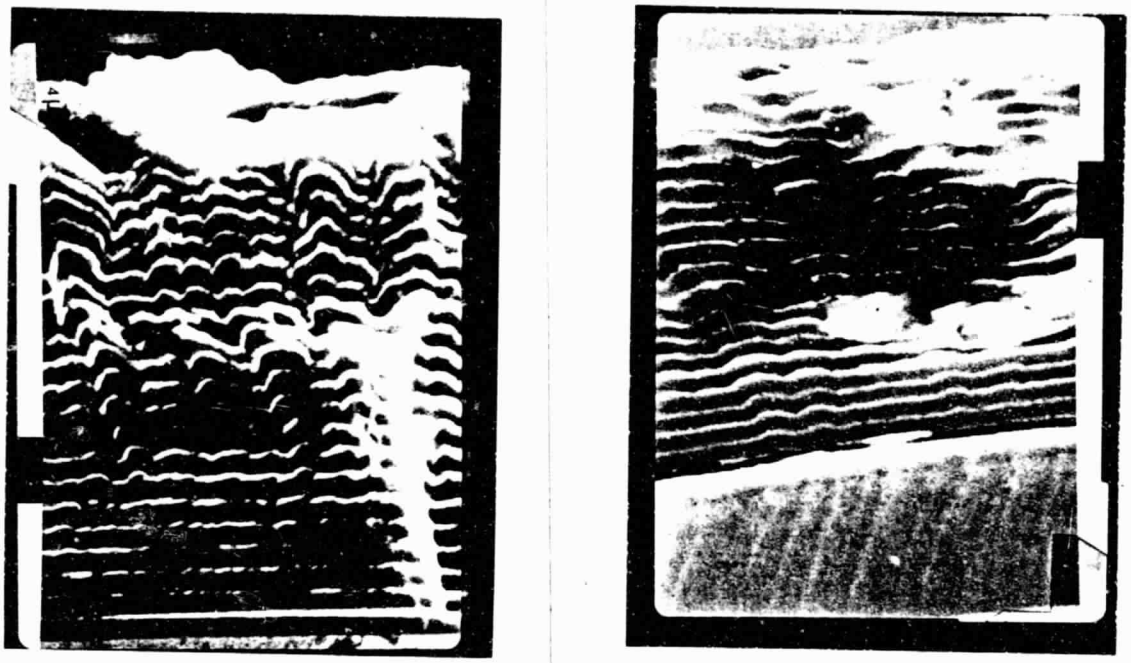
Table V. Capacitance and dissipation factor for 20 layer capacitors.

Oxide doping Main/Buffer	C microfarad	D at 1 KHz, 200 C
6%/4%	0.0911	0.05
8%/6%	0.0870	0.05

during deposition of the aluminum electrode. The new temperature of about 200°C seemed to help avoid stresses in the aluminum. Other changes such as cleaner and more carefully controlled processing were also implemented. The real proof of the success of these changes lies in the SEM micrographs. Shown in Figure 26 is a micrograph of a cross section of the 20 layer capacitor which was fabricated using the older methods along with a similiar picture for the 20 layer capacitors which we made using the improved methods. The improvement is obviously substantial. There are no longer any extreme spikes and irregularities which were previously experienced, and the general smoothness of the Upper layers is not substantially different from that of the lower layers.

The basic construction used was an improved version of the variable oxide doping technique which was mentioned in the previous report. The main idea in this method as illustrated in Fig. 23 was to create a buffer zone which has a reduced concentration of P_2O_5 in order to minimize the chemical interaction between the phosphosilicate glass (PSG) and the aluminum. Our previous attempts at a construction method of this nature resulted in excessive cracking because the buffer layer was too lightly doped. In the more recently used method, the main layer was an 8% PSG (i.e. 8% P_2O_5 in SiO_2) and the buffer layers were 6% PSG. The thickness of the buffer layer was not extremely critical and varied from about 500A to about 1000 A in thickness. The main layer was about 1μm thick.

Because much of the past research had indicated that the surface structure and irregularities were of prime importance, later research



(a) (b)

Fig. 26 (a) SEM micrograph of previous 20 layer capacitor cross section.
(b) SEM micrograph of the most recent 20 layer capacitor cross section.

concentrated on making improvements in that problem. The origin of the problem was two fold. First the quality of the PSG determined the roughness of the oxide surface. This was affected by the growth conditions of the PSG particularly the growth rate. To address that problem, we substantially lowered the growth rate in an attempt to reduce the surface roughness. Where we previously used growth rates in excess 1000 A/min, we lowered the growth rates on the first layer to 750-800 A/min and to 550-600 A/min after 5 layers. The reason for the drop in growth rate was due to the fact that the reactor was cleaned only after every 5 layers and as the reactor gets contaminated with oxide, the growth conditions are affected. The cleaning procedure is not simple and thus we settled on a procedure of cleaning after the reactor had been used 5 times.

The second major problem related to surface roughness was the aluminum electrode and the stresses which were created by the interface between the electrode and the oxide. We greatly refined the evaporation process with an improved substrate heating arrangement. The temperature at which the substrate was maintained during evaporation was increased to the range of 200-245°C. The capacitors were stored at this same temperature whenever there was a break in the fabrication sequence. The aluminum was carefully evaporated from a fixed charge of aluminum placed on the evaporation heater coil. The rate of evaporation was rather high-about 4500 to 5000 A/min giving a thickness of 3500-4000 A of deposited electr...

As a result of the improvements made in the fabrication processing there was a reduction in the surface roughness such that the number of layers was extended to 30 and the dissipation factor was improved generally over that which was previously experienced for the 20 layer devices. Shown in Fig. 27a is a photomicrograph of the surface of a 32μm PSG film made by the improved methods. Notice that the grain size is in the range of 2-4 μm which is fairly small and seems to be acceptable for 30 layer capacitors. In Fig. 27b the surface of an aluminum film 12-15μm thick is shown. This represents about 30 successive evaporation cycles of 3500-4000 A thick aluminum layers. The surface is very smooth with the average grain size being only about 2 μm or less.

1.3.7 30 Layer Capacitors

Using the above-mentioned processing sequence, successful 30 layer capacitors were contructed. As in previous multi-layer capacitors the substrate was a polished 2" silicon wafer upon which 2 μm of 8% PSG was grown as the initial layer. There was a total of 5 capacitors on the substrate arranged in a configuration shown in the photograph of Fig. 28. The dielectric area was circular with an area of about 1 cm^2. The electrodes are elongated and overlap at the edges. Figure 29 shows the masks used for the oxide on the right and the aluminum electrodes on the left. The alignment jig insured proper alignment of the two masks. A close up view of a good capacitor is shown in Fig. 30a. Note the smooth unflawed surface in contrast to the defective capacitor shown in Fig. 30b in which some cracks appeared on the surface.

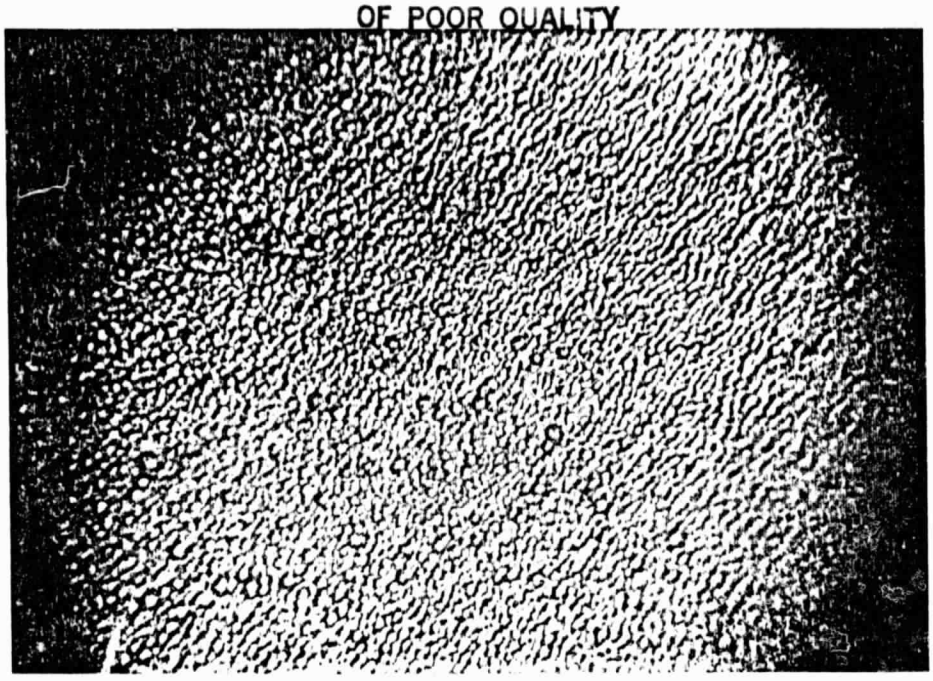


Fig. 27a Surface of a 32μm PSG film.

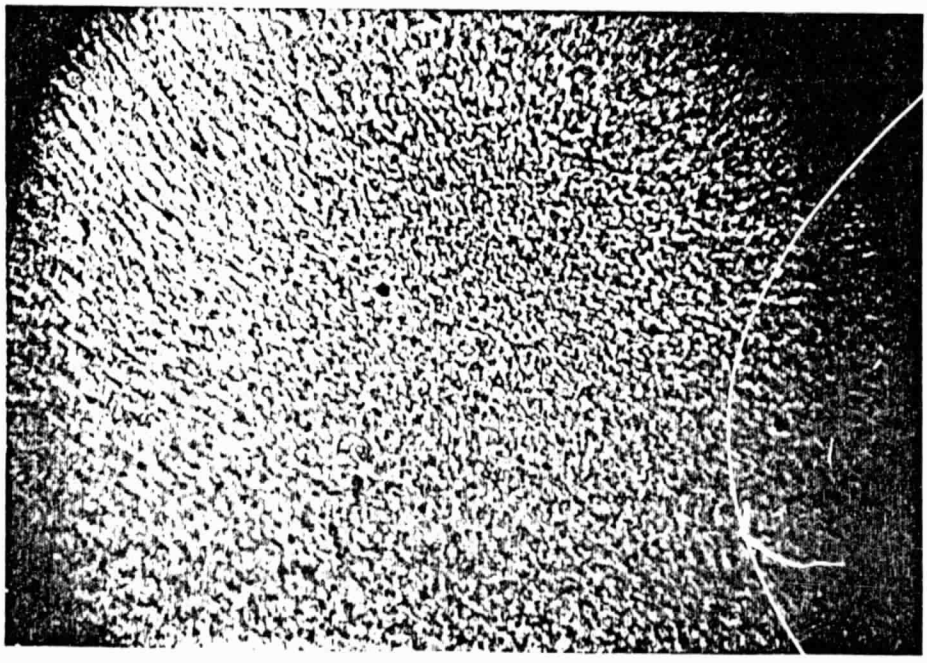


Fig. 27b Surface of a 12-15μm aluminum film.

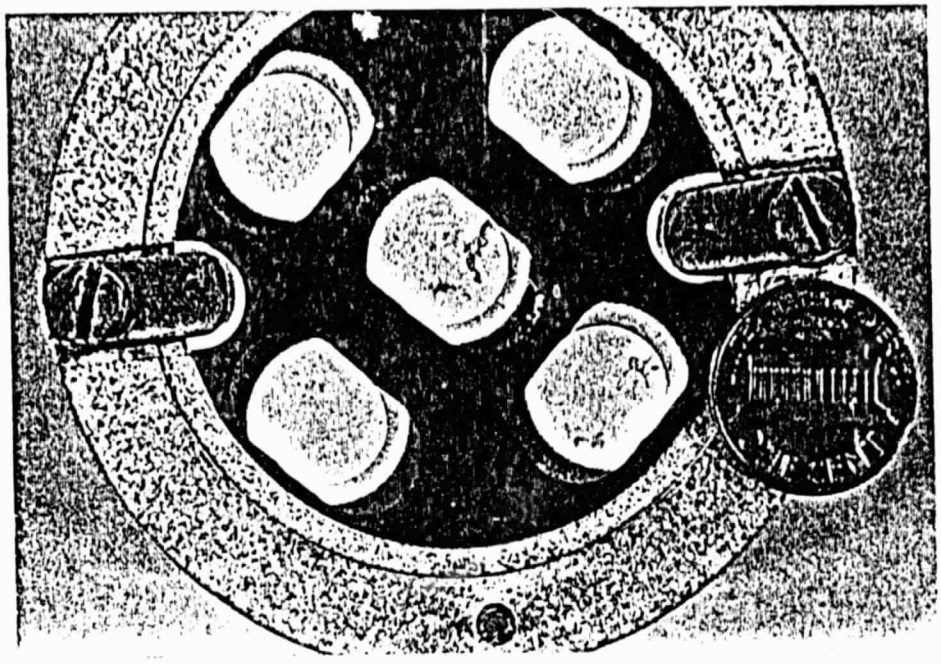


Fig.28. Slightly enlarged photograph of the 5 capacitor set.

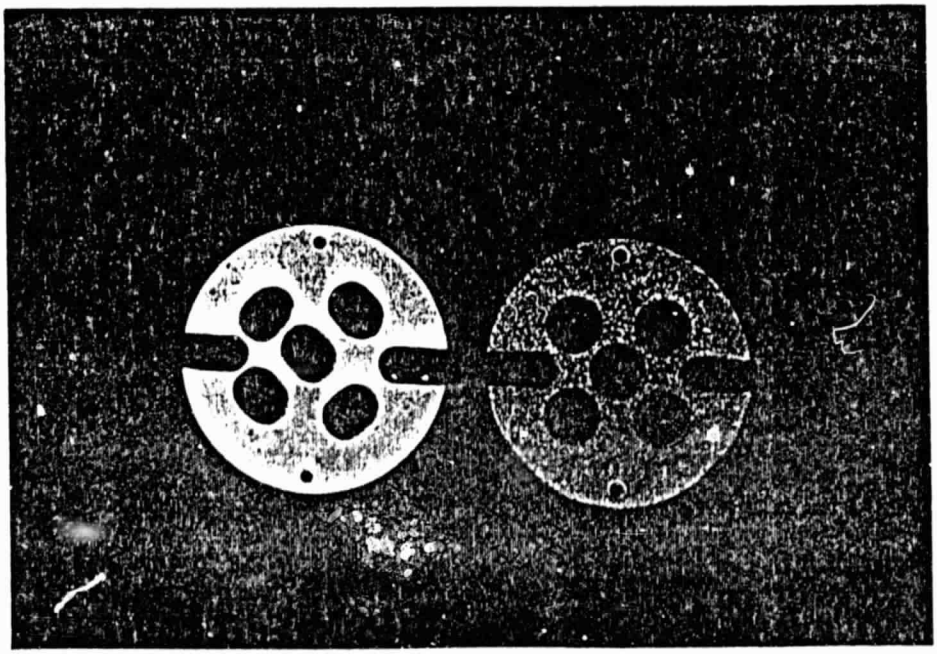


Fig.29. Aluminum mask on the left; PSG mask on the right.

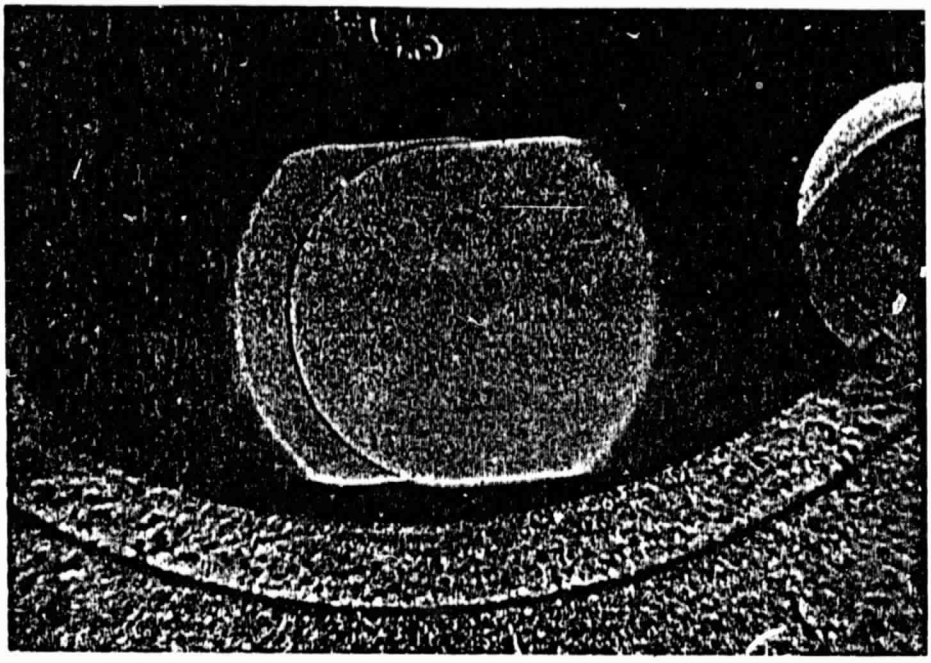


Fig.30a Close up view of one of the good capacitors.

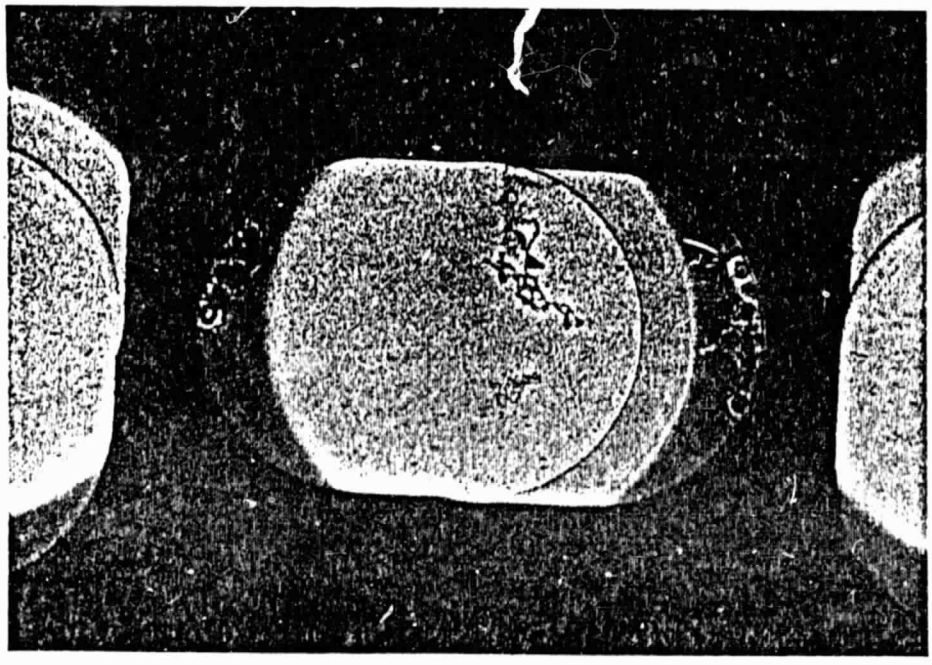


Fig.30b Close up view of a capacitor in which the surface cracked.

A high magnification (400X) view of the surface of one of the 30 layer capacitors is shown in the photograph of Fig. 31a. Note that the grain size is slightly larger than that of a 25 layer capacitor shown in Fig. 31b. For comparison the surface of a 5 layer capacitor using SiO_2 rather than PSG is shown in Fig. 31c. Because of this increase in surface roughness, it appears that additional processing steps and improvements will have to be made in order to extend the number of layers beyond the 30 which have been made to date. Occasionally there will be small defects even on capacitors which are good units. To the unaided eye they appear as small black specks. Under the microscope they have the appearance as shown in Fig. 32.

In general, the 8% PSG showed very little evidence of crack formation. There were, however, a few places where such cracks did occur. The photographs in Fig. 33 show cracks at the edge of a 30 layer capacitor. The cracks started forming in the 32 μm thick PSG and extend only to the edge of the capacitor. Figure 33b is simply a high magnification view of one of those cracks. It isn't clear exactly why such cracks form occasionally, but it is possibly due to minor defects which occur in those regions and which create additional stresses.

After every layer the capacitors were checked to see if any shorts had formed. If any were found they were blown out by discharging a 40μF capacitor which had been charged to about 70 volts through the shorted capacitor. Occasionally it is was necessary to charge the capacitor to 120 V in order to have sufficient energy to completely blow out the short. Whenever a short is blown out it was necessary to contact the electrodes with point tip probes. This resulted in appreciable electrode damage as shown in Fig. 34.

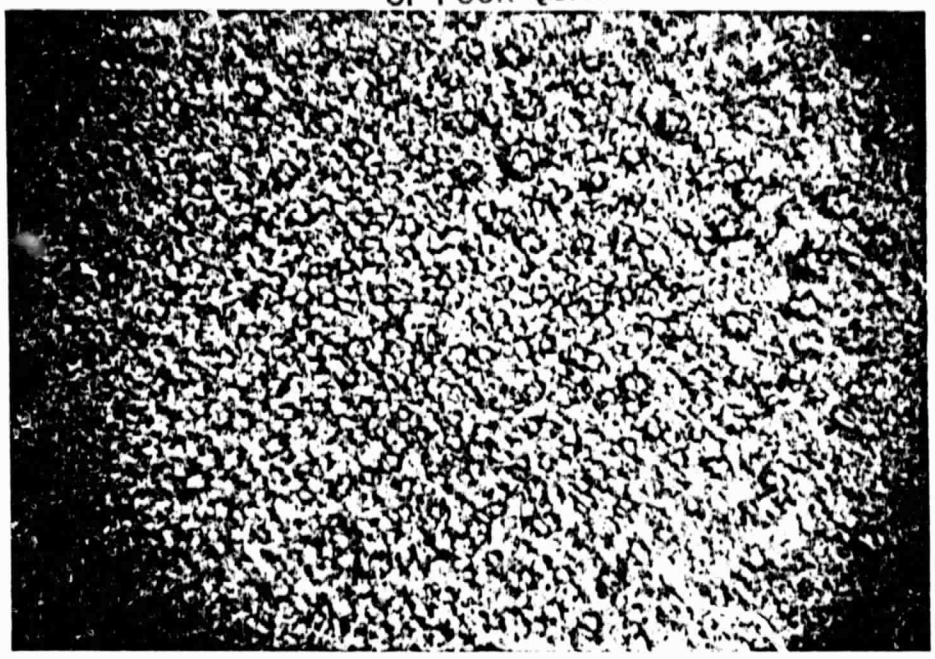


Fig. 31a Magnified view of the surface of a 30 layer capacitor.

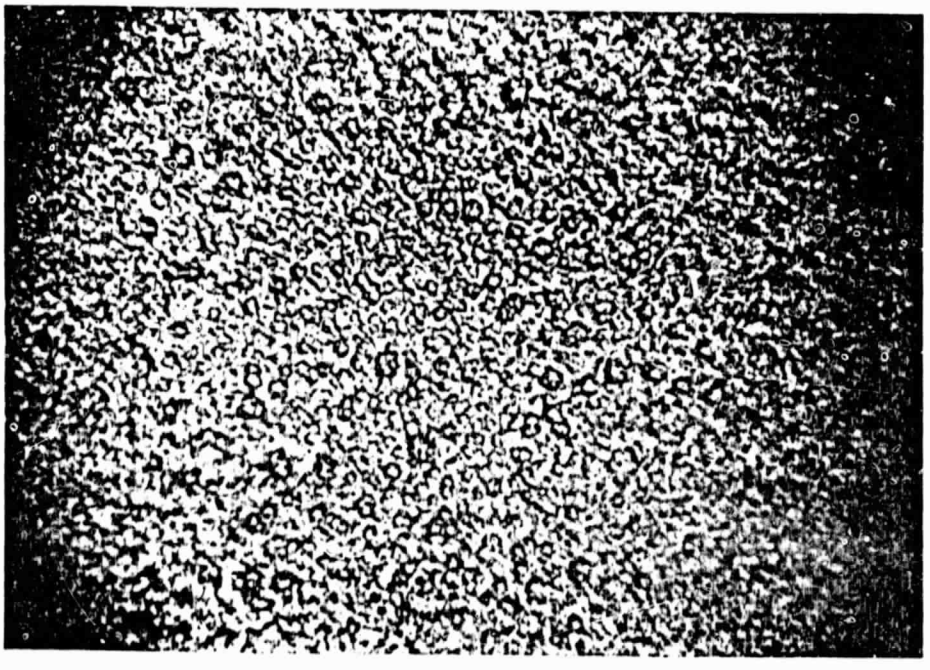


Fig. 31b Magnified view of the surface of a 25 layer capacitor.

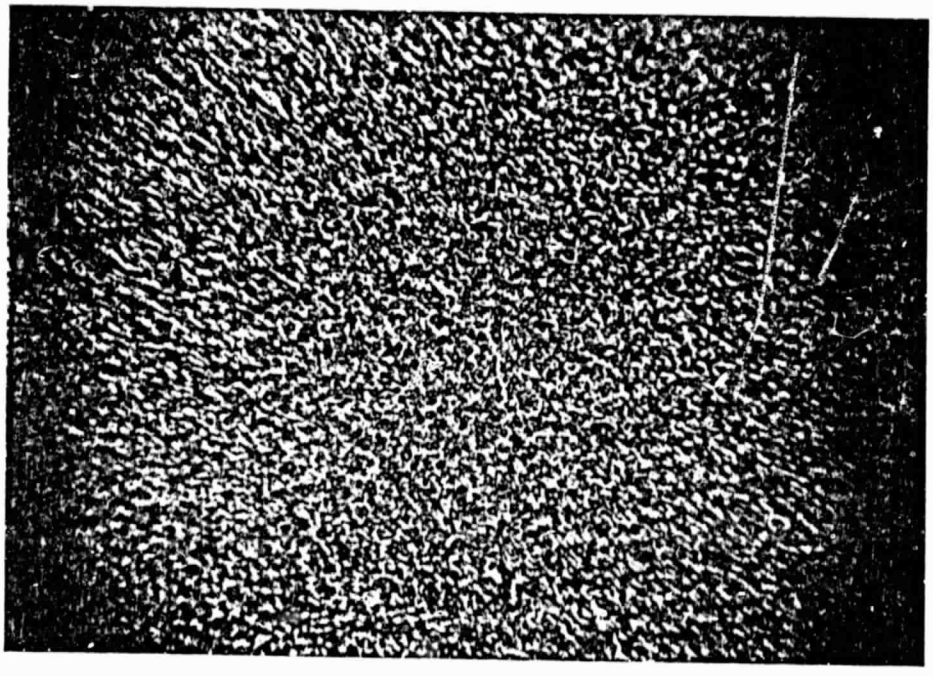


Fig. 31c Magnified view of the surface of a 5 layer capacitor.

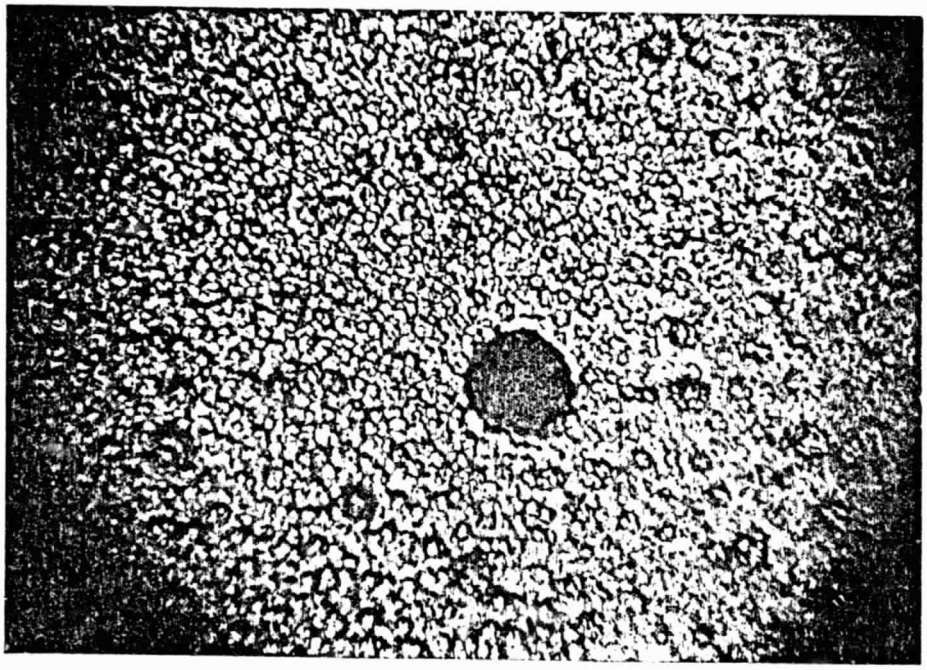


Fig. 32 Surface defect on a 30 layer capacitor.

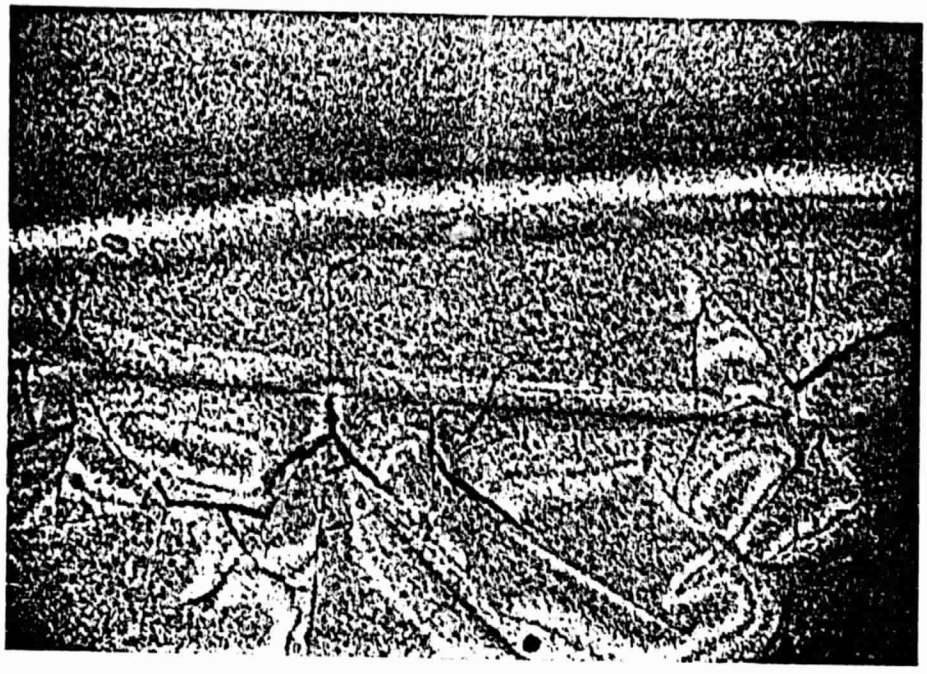


Fig. 33a Cracks at the edge of a bad 30 layer capacitor.

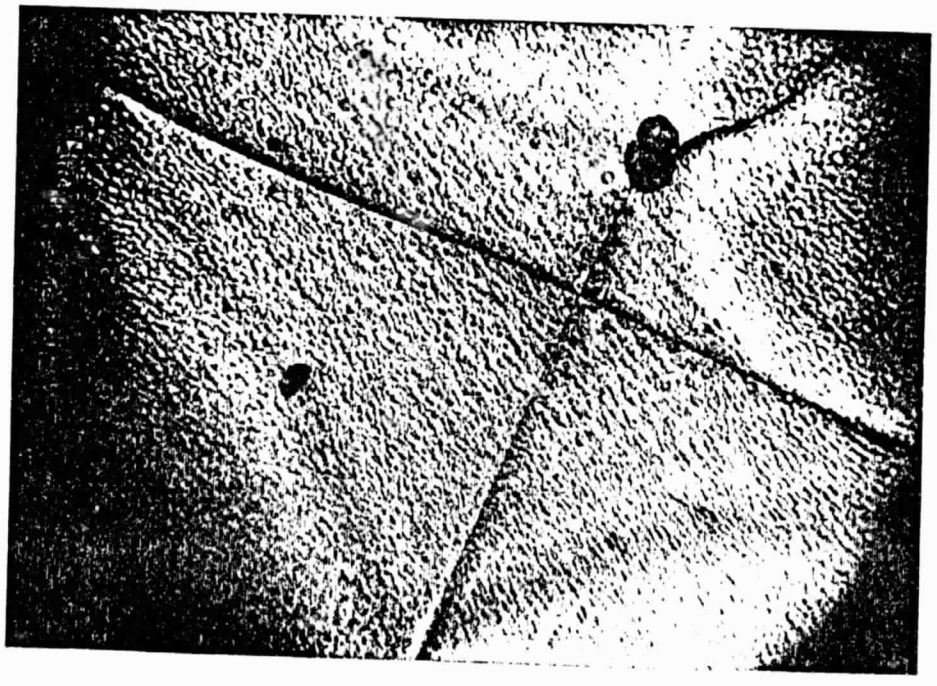


Fig. 33b. High magnification view of an edge crack.

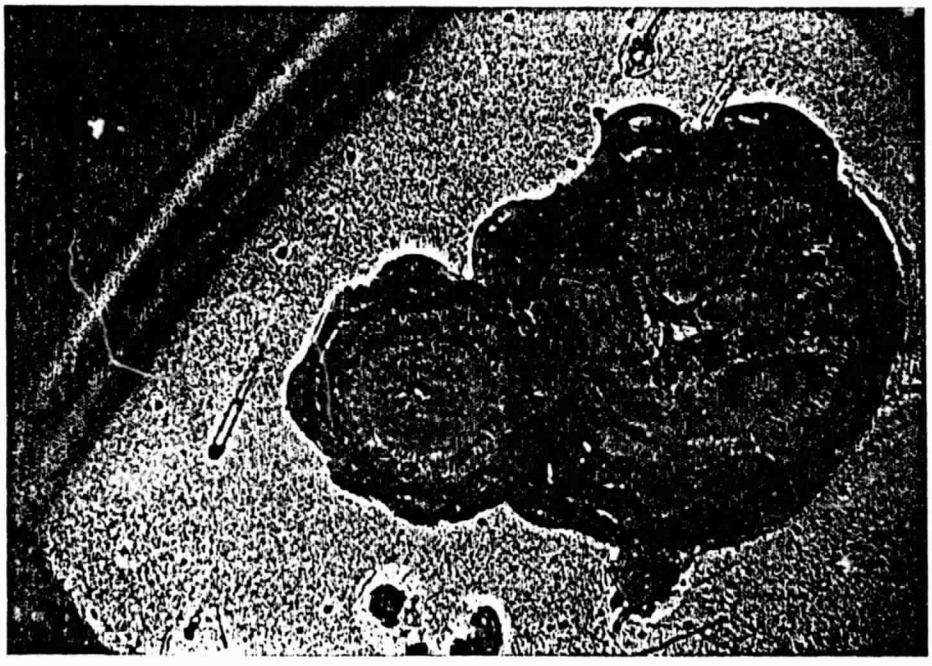


Fig. 34. Electrode damage at the contact area when shorts are blown out.

Sometimes cracks are created in the PSG by the act of blowing out the shorts. Figure 35a is a photograph of such an induced set of cracks. A higher magnification view of that is shown in Fig. 35b. In all cases when a short was blown out a pit was formed. Figure 36 shows a view of such a pit with the microscope focused on the top surface and the bottom of the pit. The measured depth of the pit was about 35-40 μm thus extending through the entire 30 layer capacitor. Such a pit would only occur when shorts in the higher numbered layers occurred.

Of the 5 capacitors which were fabricated, 3 of them had no shorts whatever and did not require any blowouts. The 4th capacitor was shorted only once, that occurring on the 28th layer. The 5th capacitor was very bad, giving rise to shorts on 10 different layers. Thus overall the process sequence was really quite good. There were, unfortunately, shorts which formed even in the good capacitors after they had been stored for about 3 weeks. This long term failure problem was not understood. However it is possible that moisture absorption into the PSG could have been the cause of this. It was possible to blow the shorts out but this resulted in a substantial increase in the dissipation factor.

The capacitance of the good capacitors was exactly what was expected from the theoretical value, namely about 0.18 μF. Shown in Fig. 37 is a plot of the capacitance as a function of frequency for one of the good capacitors. The data beyond 20 kHz is probably inaccurate due to the limitation of the impedance bridge. It is not likely that the true capacitance shows such a radical increase. The impedance

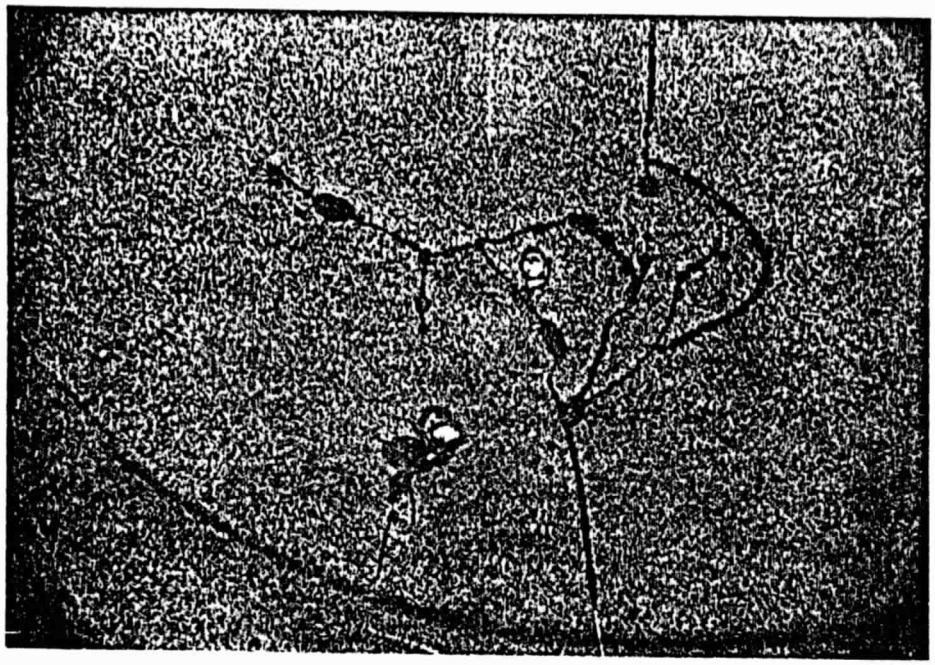
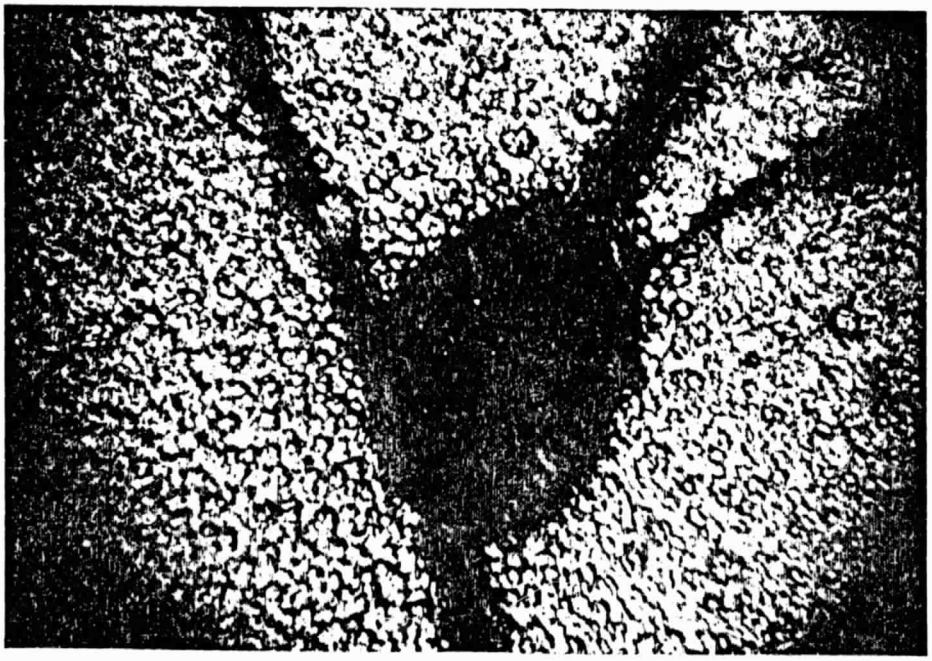


Fig. 35a Cracks induced by blowing shorts.



25μm

Fig. 35b Close up view of induced cracks.

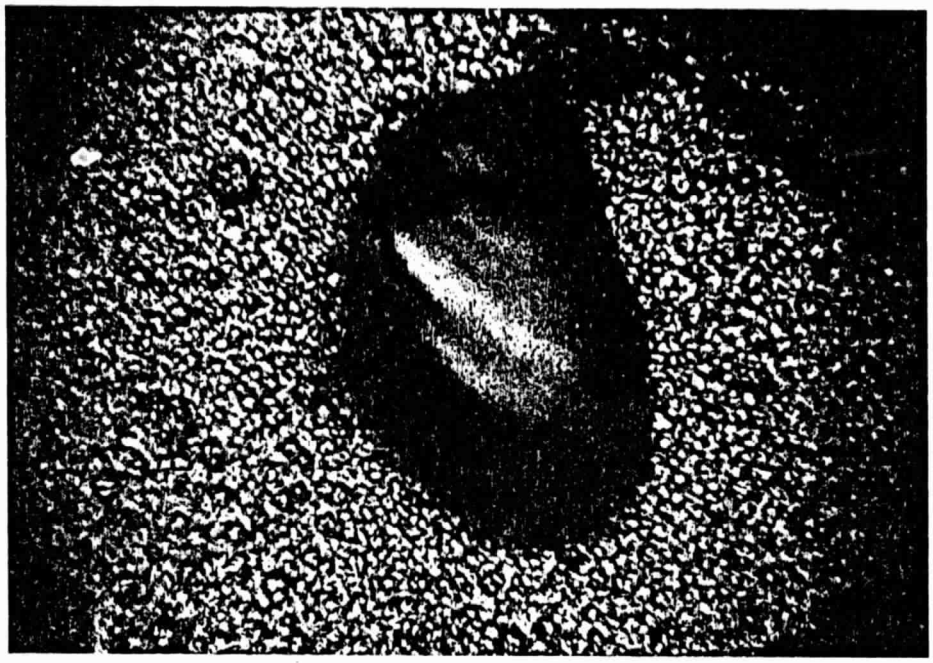


Fig. 36a Pit created by blowing a short. (Focussed on the top).

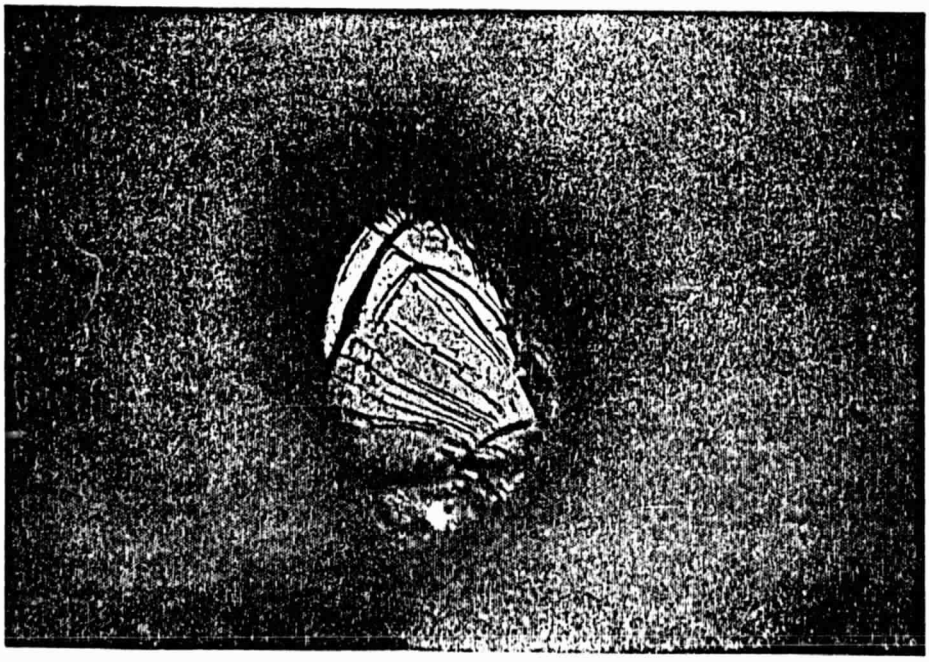


Fig. 36b Pit created by blowing a short. (Focussed on the bottom).

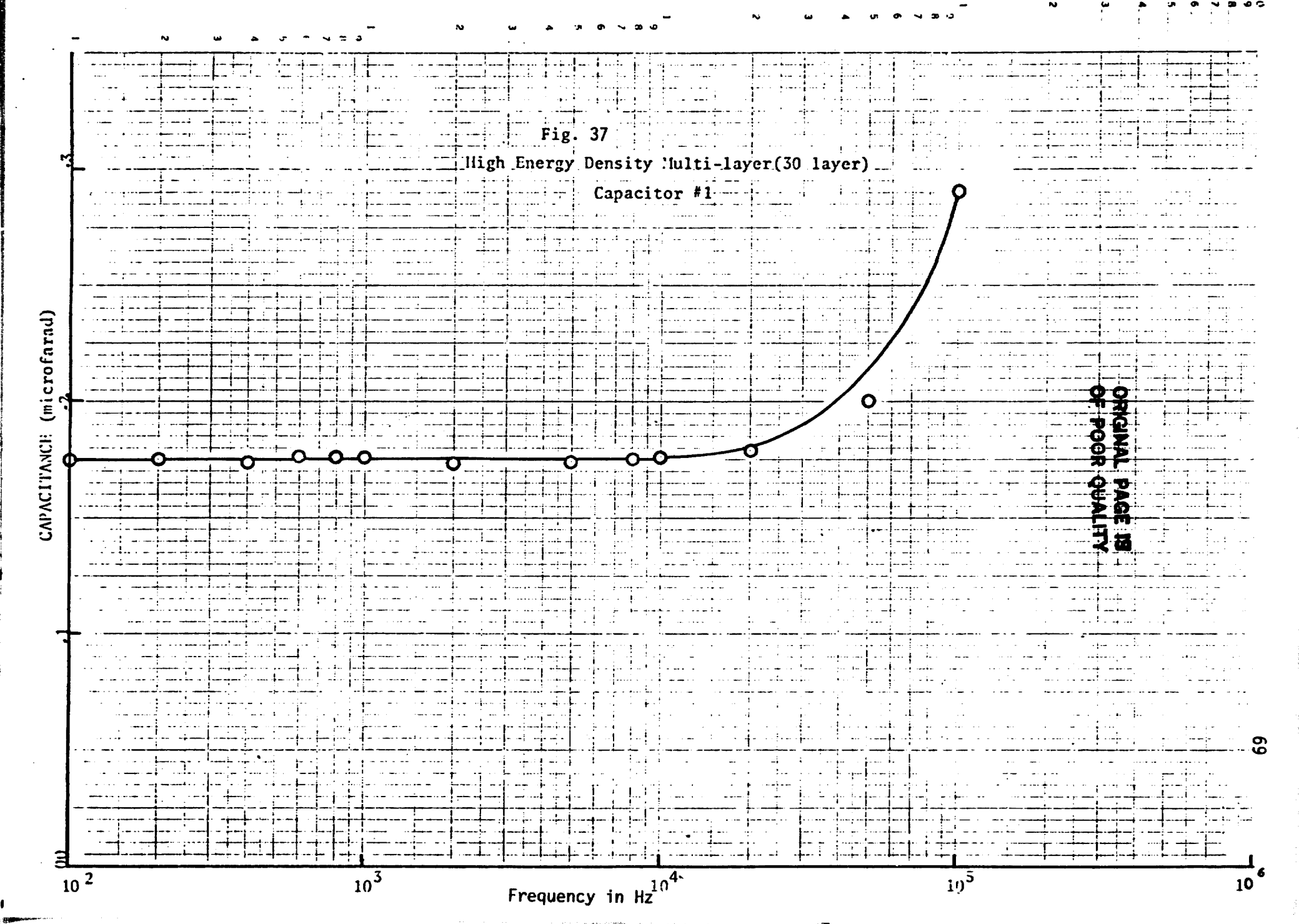


Fig. 37
High Energy Density Multi-layer(30 layer)
Capacitor #1
CAPACITANCE (microfarad)
.3
.2
.1
0
10^2
10^3
10^4
10^5
10^6
Frequency in Hz
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bridge accuracy is only guaranteed up to 20 kHz. The dissipation factor of this same capacitor is plotted in Fig. 38. At low frequencies the dissipation factor is reasonable but it rises to rather high values at 100 kHz. The scatter in the data is due mainly to the fact that the impedance bridge is not very sensitive to dissipation factor changes and hence the accuracy is not very good.

The effect of temperature variations upon capacitance and dissipation factor were also studied. Shown in Fig. 39 is a curve of the capacitance as a function of temperature for one of the capacitors. In general although the capacitance did not vary linearly with temperature it could be assigned a temperature coefficient of about +100pmm/C which is quite small.

The dissipation factor for one of the capacitors is plotted in Fig. 40. The increase at higher temperatures is due to the increased leakage through the dielectric.

There was quite a bit of change in the surface of a multi-layer capacitor as the number of layers was increased. In general the roughness increased which led to increased shorting probability. Another effect was observed, namely that of the upper oxide layers becoming thinner. The reason for that wasnot well understood although we made a guess that the surface temperature was lower as each layer was added, resulting in a reduced growth rate. This effect was first observed as an increase in the capacitance per layer for the higher numbered layers. Shown in Fig. 41 is a plot of the capacitance per layer as a function of the number of layers. These data were calculated from changes in the

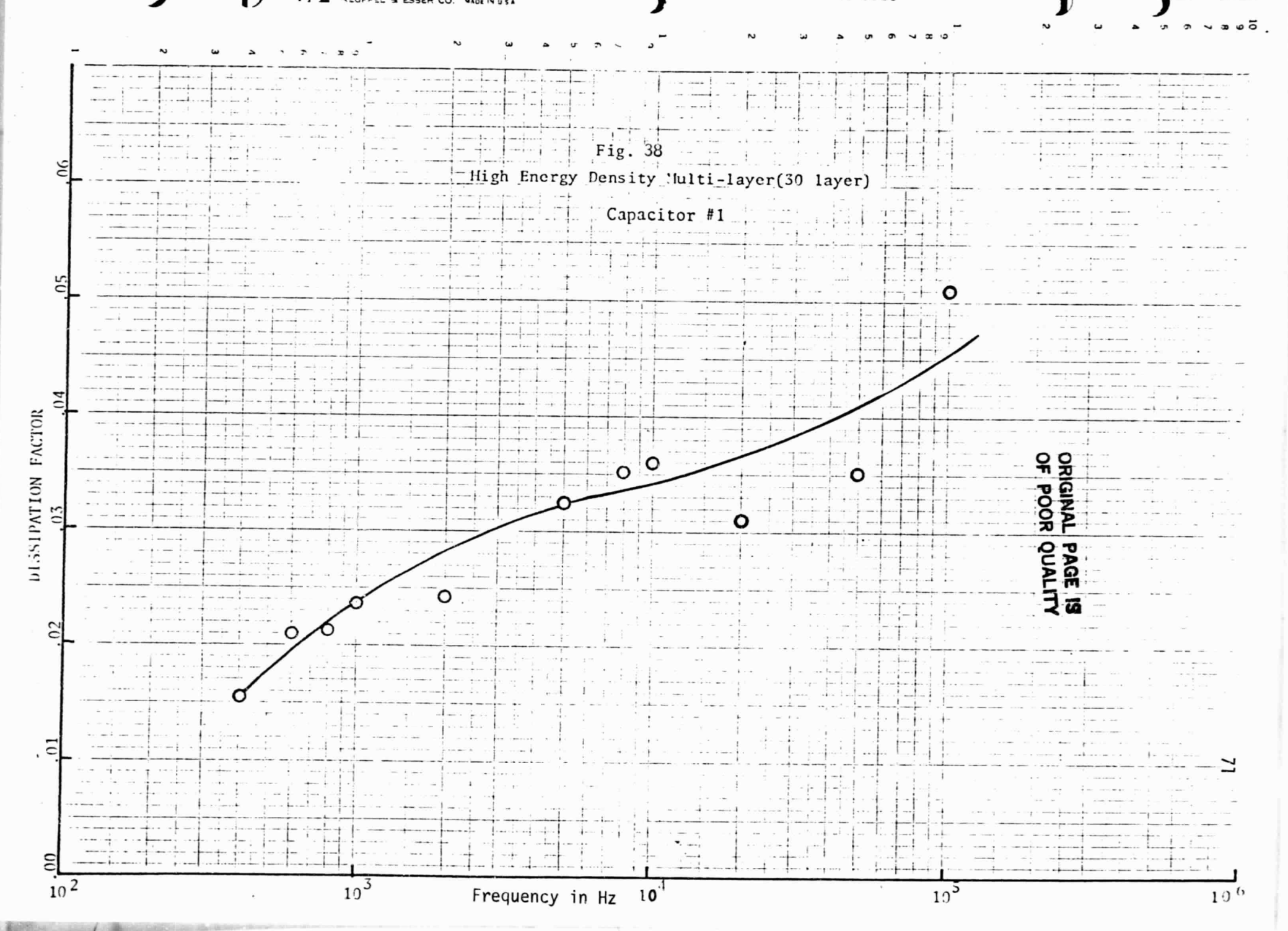
Fig. 38
High Energy Density Multi-layer(30 layer)
Capacitor #1
DISSIPATION FACTOR
.06
.05
.04
.03
.02
.01
.00
10^2
10^3
Frequency in Hz
10^5
10^6
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71

Fig. 39

High Energy Density Multi-layer (30 layers)
Capacitor #1

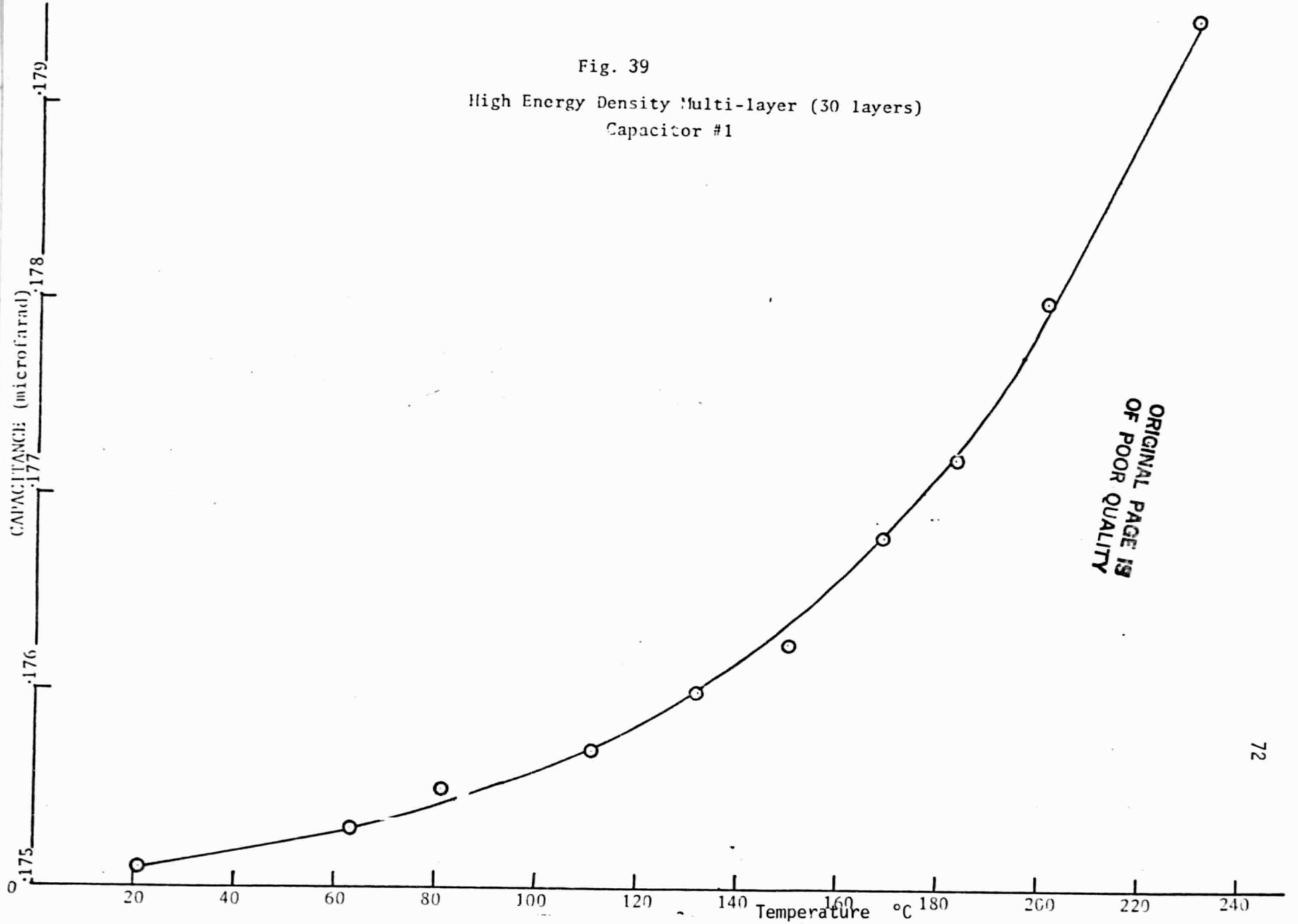


Fig. 40

High Energy Density Multi-layer (30 layer)
Capacitor #1

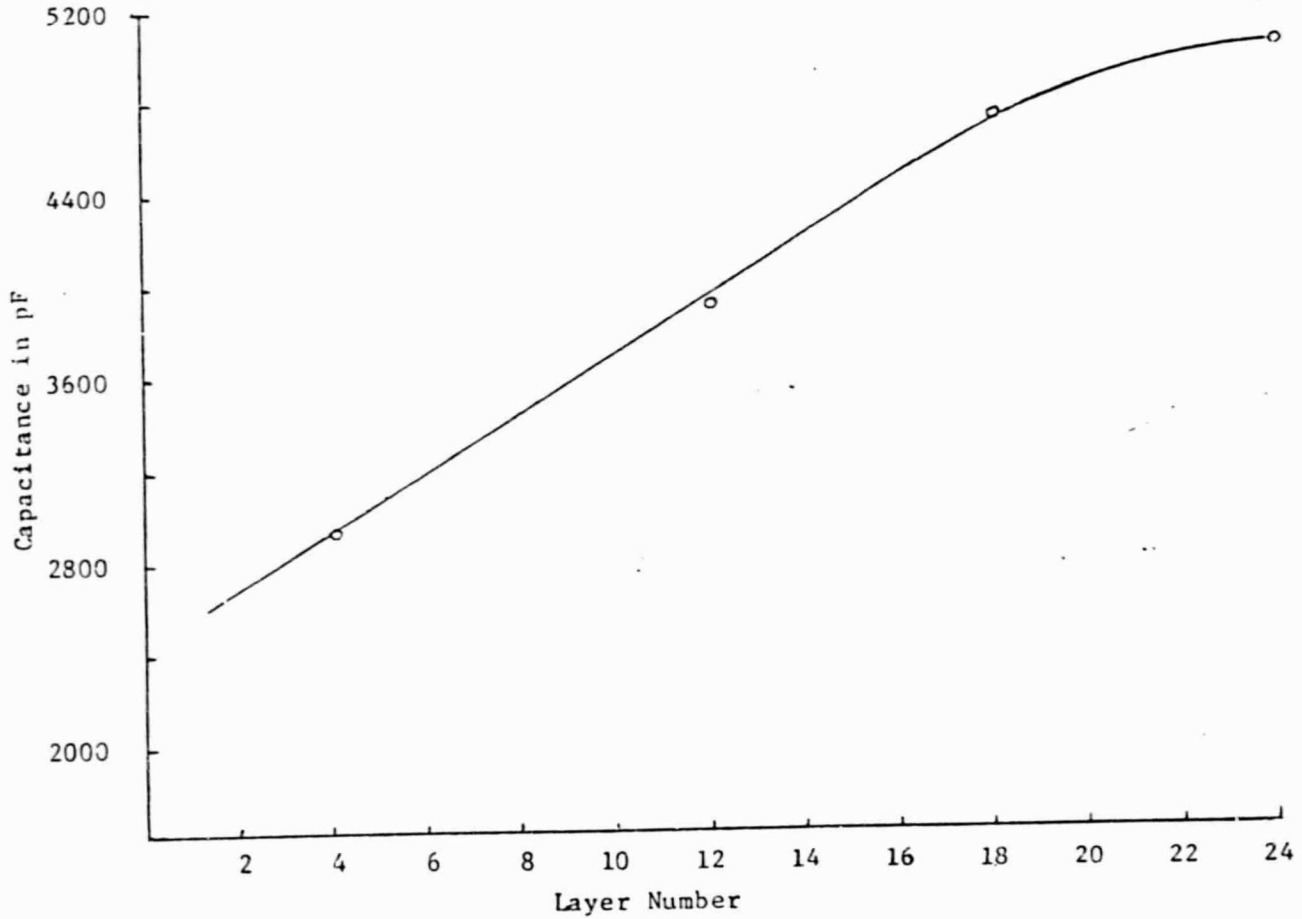


Fig. 41 Capacitance per layer as a function of layer number for a multi-layer capacitor.

capacitance after several layers had been deposited. The amount of increase is not negligible as can be clearly seen. Essentially the thickness had been cut in half for the upper layers.

A detailed examination of the thickness of each layer was made using an SEM photograph of the cross section of one such capacitor. The results of those measurements are shown in the plot of Fig. 42. The trend is a steady decrease in layer thickness although there are some regions of temporary increase. These are probably due to the points in time where a new group of layers were added. Usually only about 4 to 6 layers were deposited during any one work session. After that it was at least one day and perhaps several days before the next group of layers was deposited.

Some experiments were run to try to measure the surface temperature and to increase the temperature as the number of layers was increased. That did seem to indicate that the problem was related to surface temperature at least somewhat. However the results were difficult to interpret and hence the conclusions are not assured. In order to maintain a reasonable thickness at the upper layers, the growth time was extended to compensate for the reduced growth rate.

The fact that thinner layers were experienced is even more crucial as the roughness increases. Figure 43 shows surface and cross section SEM views of a 32 layer capacitor structure. The formation of these nodules from which the growth propagates makes it very difficult to maintain high integrity in the insulating layer. Thus it became of even greater importance that the thickness of the upper layers be at least as great as those of the lower layers.

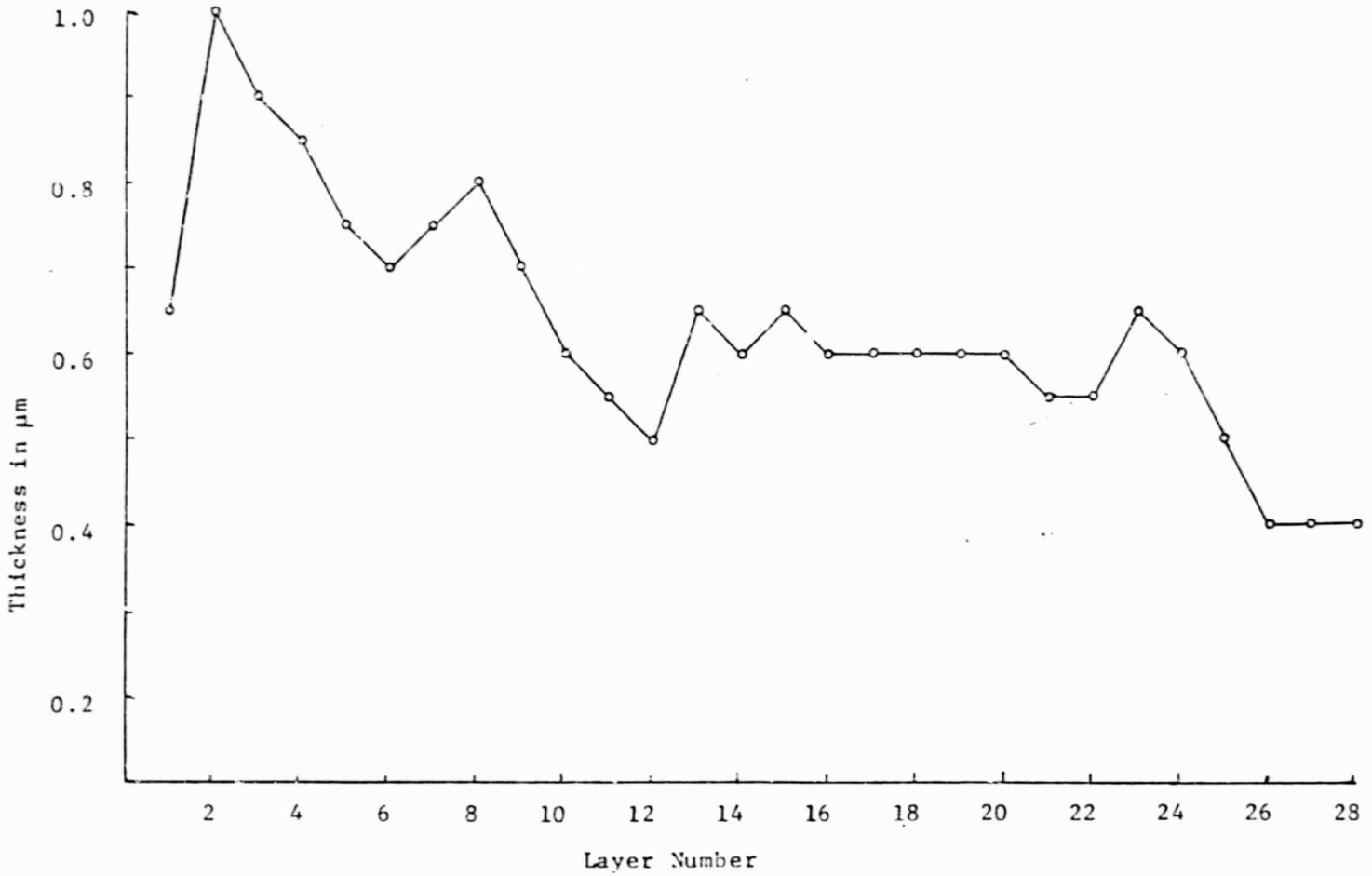
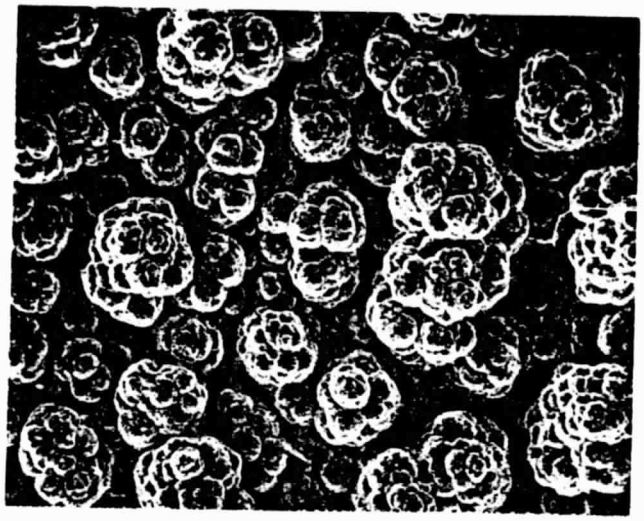
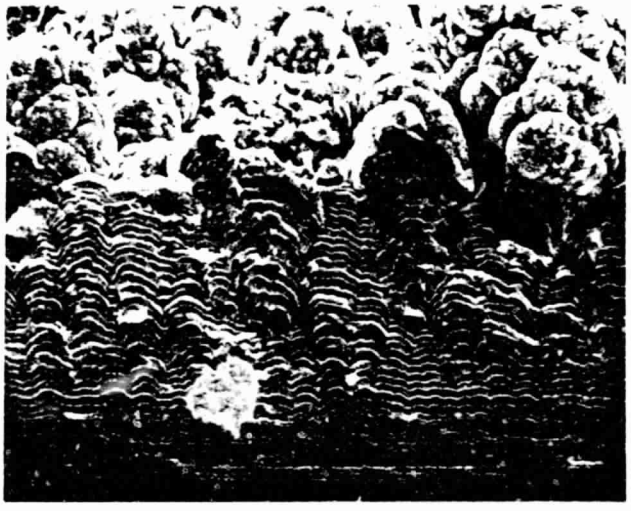


Fig. 42. Thickness per layer as a function of layer number for a multi-layer capacitor. The thicknesses were estimated from an SEM photograph.



a



b

Fig. 43. (a) SEM photo showing the surface view of a 32 layer capacitor structure in which the nodules are clearly evident.
(b) SEM cross section of the same capacitor. Note how the nodules propagate upward & increase in size as layers are added.

1.4 SPIN-ON PHOSPHOSILICATE GLASS

A spin-on source PSG is an alcohol solution of a phosphosilicate glass such that the source is applied by spinning, dipping or spraying the solution. Upon drying in order to drive off the volatiles, the result is a glass film with characteristiccs quite similar to that of deposited PSG. The manufacturer, Emulsitone Company, did not give an indication of the amount of phosphorus pentoxide in the film but it was suspected that it was less than the 6-8% which we used in the pyrolytically deposited PSG. We did not run infrared absorption curves to determine the concentration.

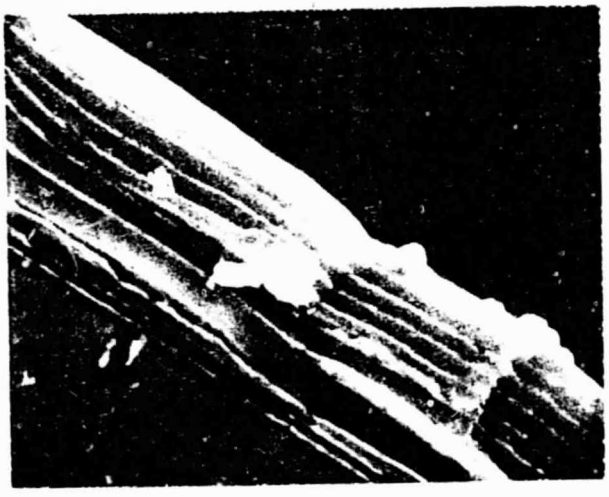
In order to begin the process of evaluation of this new type of source, three experiments were done in order to get an idea of the characteristics. The first of the tests was an attempt to determine whether or not the surface roughness problem could be improved by the use of such a spin-on source. The procedure used was to spin on either one, two or three coats of the PSG following each coating with an anneal step which was a 15-20 minute bake at 400°C. Then a layer of aluminum was evaporated on top to aid in viewing with an SEM. The results were examined using an SEM. It seemed quite clear from the SEM pictures that the spin-on source was in fact helping to accomplish its primary objective, which was to reduce the surface roughness. Unlike the gas phase pyrolytically deposited PSG, the liquid spin-on source tended to fill in the valleys and as a result the surface was smoother after such a deposition. This was very encouraging since it offered some hope for a procedure to solve the long standing difficulty associated with the sur-

face conditions. Naturally there was still the question of possible cracks forming in such a spin-on layer. In addition there was the problem of masking the electrodes during the spin-on operation. We could not use a convenient mechanical mask as we employed for the gas phase operations because of the problem of shadowing of regions beyond the electrodes. Thus the spin-on approach did present some new problems even if it did help solve other problems.

The second experiment performed was to make a several layer capacitor using only spin-on PSG, without any pyrolytic PSG. In order to simplify the construction, no masking was done and it was thus not possible to measure capacitance since the proper electrodes could not be accessed. What it did tell us,, however, was the nature of a multilayer spin-on structure when a cross section view is taken of it using an SEM. In Fig. 44 are shown cross sections of a seven layer structure made with spin-on PSG. Several features are significant to note. The uniformity of thickness is reasonably good from one layer to the next. Especially important is the fact that where surface particles or defects have appeared such as in Fig. 44a, the successive layers have actually reduced the resulting surface irregularity rather than magnified it as would be the case with the gas phase chemical vapor deposition of PSG. This again was an encouraging sign and pointed toward some possible improvements through the use of the spin-on source.

However, the photographs also point out a problem or two. The large defect which appears at the left side of Fig. 44a is something that is peculiar to the spin-on source. Defects of that size were not

a



b

Fig. 44 a,b SEM photos of the cross section of a 7 layer capacitor using only spin-on PSG as the dielectric.

previously noted with CVD PSG. In order to take a better look at such defects, a surface view under low magnification was made of the multi-layer spin-on structure. This is shown in Fig. 45. The crystallites on the surface are apparently a result of the processing used for spin-on deposition and drying. We ran some experiments on variations in the drying procedure and were able to produce some improvement in this situation.

The third experiment which was performed using the spin-on source was the construction of a standard pyrolytically deposited multi-layer structure but with the addition of a spin-on layer once every six or seven layers. The idea of this approach is to determine whether or not such a layer could help reduce the surface irregularity problem. Thus a 25 layer capacitor was made in which the 6th, 13th and 22nd dielectric layers were augmented with a spin-on PSG layer. On those layers the normal pyrolytic oxide was first deposited followed by a thin, approximately 2000A, layer of spin-on oxide. Thus it would not be expected that the spin-on layer would be enough to completely fill in the valleys but some improvement should be noted. Figure 46 is an SEM picture of the cross-section of that capacitor with the layers which have the spin-on oxide added marked with arrows. Although careful inspection is required for discerning the results, it is clear that the layers which have spin-on oxide added are smoother than the immediately preceding layer.

The capacitance and dissipation factor were measured as a function of frequency for this hybrid capacitor which used the three spin-on

Fig. 45. Surface view of the spin-on PSG multilayer capacitor illustrating the formation of crystallites due to an imperfect drying procedure.

Fig. 46. SEM photo of the cross section view of a 25 layer capacitor in which the 6th, 13th and 22nd layers (marked with arrows) have a spin-on PSG layer added to help reduce the surface roughness.

layers. The dissipation factor was somewhat higher than we would have liked but it is not too bad at low frequencies. As with the other capacitors, the dissipation factor increased with increasing frequency indicating that the series resistance of the aluminum electrodes was limiting the dissipation and not the shunt leakage through the oxide.

2. POLYMERS AS DIELECTRIC MATERIALS

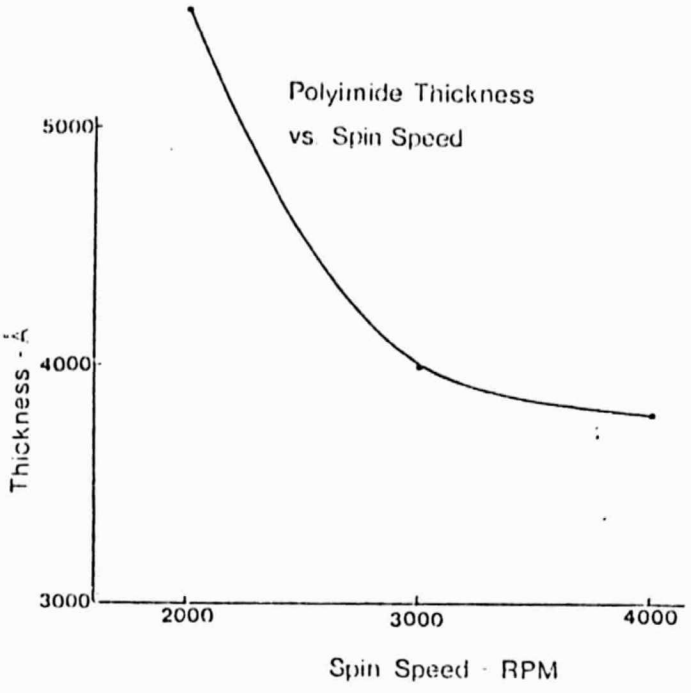
2.1 POLYIMIDE

Although silicon dioxide has a number of advantages as a dielectric, it also has a number of problems as we have noted. It was with these limitations in mind that we decided to direct our research efforts to a slightly new direction in an attempt to look at different materials for use as the capacitor dielectric.

Polyimide seemed to be an ideal choice for this role. It has recently become available in electronic grade material and seems to possess some excellent characteristics relative to the needs in this work. It has a very high tensile strength and elongation and yet is flexible enough for a thin film to be bent 180 without breaking. It's electrical characteristics were good insofar as breakdown voltage and dissipation factor were concerned. The volume and surface resistivities are quite high. The only disadvantage is a relatively low dielectric constant, about 3.5. This however is not that much lower than the dielectric constant of silicon dioxide which is about 3.9.

It can be applied by spinning which means that layer thicknesses of 1 μm or less can be achieved. We made a number of measurements on the thickness as a function of spin speed and number of applications, the results of which are shown in Fig. 47. These results already show that the polyimide thickness can be controlled in the ranges which are of interest in this work.

Curing time and temperature were found to be important in the determination of the film thickness as well as other important



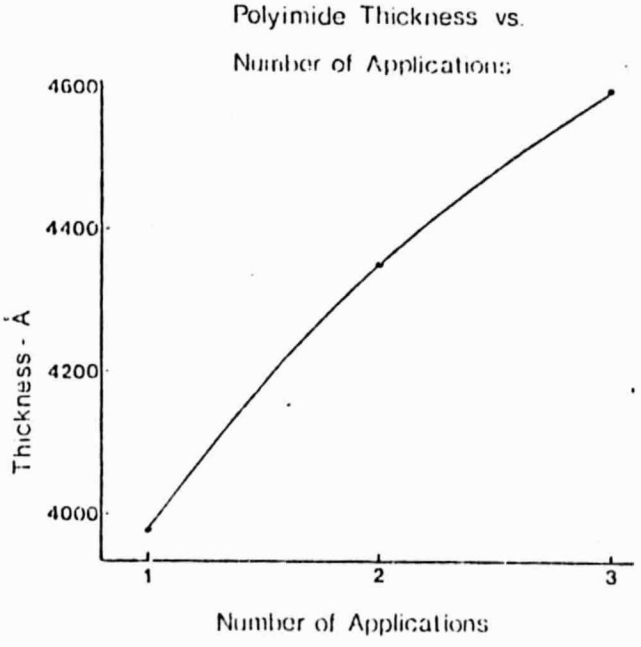


Figure 47 . THICKNESS VARIATION OF POLYMIDE WITH SPIN SPEED AND NUMBER OF APPLICATIONS PER LAYER.

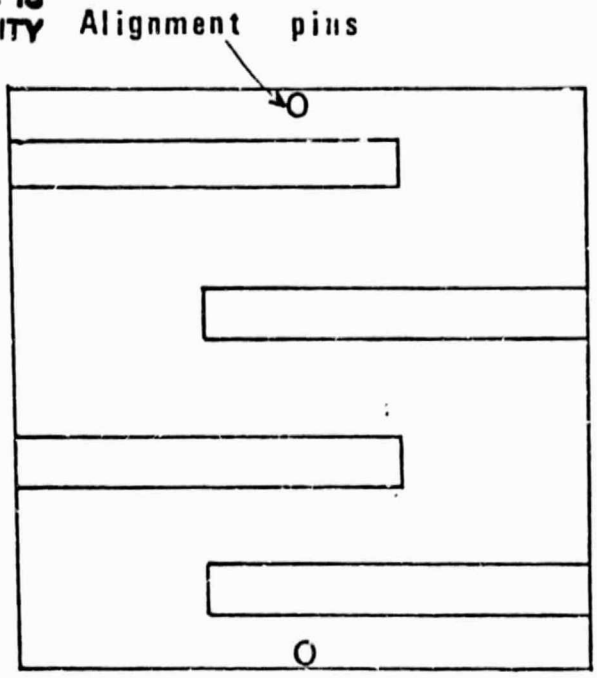
characteristics. A final cure cycle of 350°C for 30 min. was selected for most of this work. We found it to be of extreme importance to filter the polymer immediately prior to dispensing to reduce particulate matter problems which is one of the causes of pin holes in the film. Filter sizes down to .5 μm were used.

The multilayer capacitors were fabricated by alternating layers of polyimide and evaporated aluminum on a photographic glass plate substrate, the High Resolution Plate (HRP) manufactured by Kodak, Inc. The HRP plates were selected because of the flatness of the surface on the emulsion side and their ability to withstand the temperature cycling. To prepare the HRP plates for use as substrates several cleaning steps were necessary. The emulsion was stripped off by immersing the plate in a 5% solution of hydrofluoric acid (H.F.) and dionized water (D.I.) for 15 seconds. Care was taken not to exceed this time because the hydrofluoric acid attacked the glass and ruined the smoothness. The plate was then placed in a running D.I. bath followed by a hydrophobic and a hydrophilic cleaning, a separate three minute immersion in boiling trichloroethylene (TCE) and boiling acetone being suited for this purpose. The plate was then rinsed in running D.I. for three minutes, placed in a 2-propanol (isopropyl alchohol) bath for thirty second, and blown dry with filtered nitrogen.

Once the plate was cleaned, a layer of polyimide was spun on because the aluminum adheres better to the polyimide than the glass. In order to apply the polyimide to the glass plate is was necessary to use the adhension promoter VM 651, as manufactured by DuPont and reduced to

a .1-.01% concentration with methanol for application. The coupler was filtered using the same technique as with the polyimide, and once reduced was discarded after five days. With the initial coat of polyimide applied, the HRP was placed on a hot plate which was set at 350 °C for 30 minutes and which was kept on a laminar flow clean bench. The plate must be kept enclosed at all times when not on a clean bench as the uncured polyimide has a strong affinity for particulate contamination.

Using the initial layer of polyimide as a base, the plate was ready for the first metalization. This is when the capacitor pattern is delineated by using a metal shadow mask in the aluminum evaporator. The capacitor pattern and a cross-sectional view are illustrated in Fig. 48. The evaporation was done in a minimum vacuum of $5x10^{-6}$ Torr using 99.96% pure aluminum wire on a tungsten spiral wound wire filament. Discretion was exercised in monitoring the deposition rate. High deposition rates at good vacuums result in the purest film. However high deposition rates also result in a phenomenon called microsplatters which is caused by the molten aluminum outgassing during the vaporization stage. This causes small masses of molten aluminum to shoot off of the filament before it is vaporized and is characterized by small projections off the evaporated aluminum surface. This can be remedied by using specially prepared gas-free aluminum or by moderating the deposition rate to an experimentally determined acceptable level. The aluminum film thickness must be at least 4000A thick in order to maintain the bulk resistivity value.



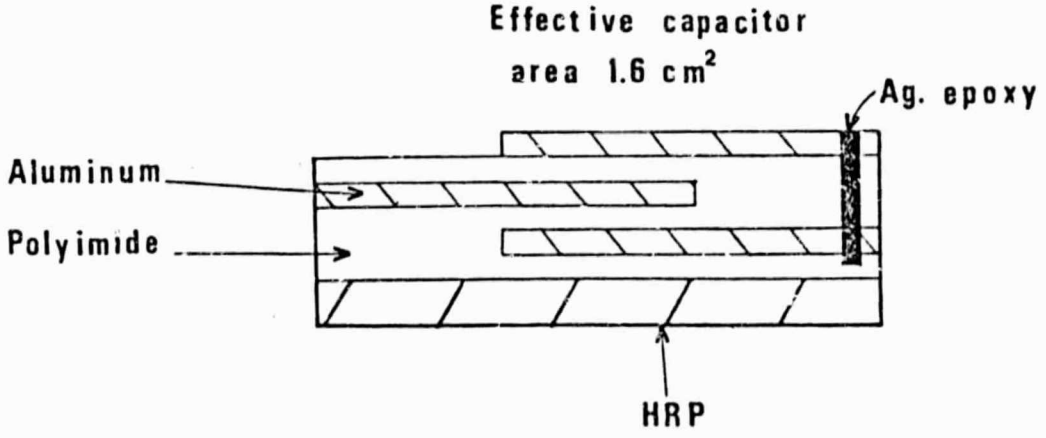


Figure 48 . TOP VIEW AND CROSS SECTIONAL VIEW OF CAPACITANCE STRUCTURES.

The dielectric layers were placed between the alternating layers of electrodes. Each layer was comprised of two spun-on layers, spun directly on top of each other without a curing cycle in between. The polyamic solution used was reduced 50% with the appropriate thinner T-8035 as manufactured by DuPont, therefore the resultant double application layer was approximately 4000A thick as shown in Fig. 47. The reason for the double application per layer technique was to minimize pinholes. The only quantitative method available to discern the density of pinholes was simply to process several batches of one application, two applications, and three application per layer capacitors. There was a significant difference in pinhole density between the single and double applications but no significant improvement in the triple application per layer capacitors. Therefore the double application method was selected because of its thinness. Several authors have reported on a reverse carbon decoration process for the delineation of pinholes and have noted densities of 5 cm^{-2} and .1cm^{-2} with 1 and 3 μm thick films respectively. One problem with dispensing the polyamic acid that was noted was the presence of air bubbles that result from forcing the solution through the filters. This was especially troublesome when using the polyamic acid undiluted because the high viscosity of the solution retarded the rise of the bubbles to the surface where they were spun off. To rectify this, an infrared light source was used to heat the polyamic acid for about thirty seconds after it was pooled on the substrate. This warming of the liquid temporarily decreased the viscosity and allowed the bubbles to rise to

the surface. When using reduced polyamic acid, a brief ten second wait allowed the bubbles to rise on their own accord.

The most successful capacitor made using the aforementioned processing techniques and materials was a ten layer capacitor. The limiting factor was a bubbling phenomena that affected the composite structure and manifested itself anytime from the fourth layer on, as shown in Fig. 49. This blistering occurred only during the cure cycles and was caused by the mismatcch in the thermal coefficients of expansion between the glass substrate and the aluminum electrodes. Although the coefficient of expansion of the polyimide is comparable to that of aluminum, very little stress occurs in the polymer due to the considerably lower modulus of elasticity in the polyimide. This has been verified by tests which include making a thirteen layer structure on a substrate of aluminum at a curing temperature of 400°C to further strain the device. The capacitor showed no signs of the slightest bubbling. The bubbling had also occurred at earlier stages in this research, at the first and second applied layers, but this was due to a surface skin effect caused by curing in an oven. The surface of the polyimide would form a surface skin first due to the ambient temperature, and when the bulk of the film cured, the water vapor given off was trapped by the surface skin creating bubbles. These are the reasons that the heat curing was done on a hot plate at 350°C. The minimum cure temperature needed to insure a fully cured film, which means the completion of the imide carbonyl bond, is 250°C as determined by infrared absorption analysis. The maximum cure temperature in air is approximately 480°C while in a nitrogen ambient it is 525°C.

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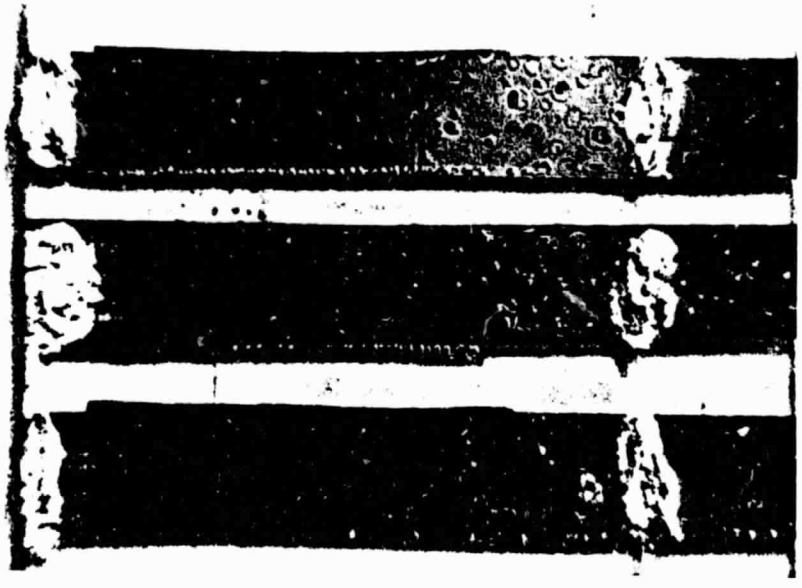


Fig. 49. Blistering effect caused by the mismatch in the coefficients of thermal expansion.

Since the bubbling problem was a direct result of the mismatch in the thermal expansion coefficients, several other substrates were investigated. The specifications for a substrate are that it be an insulator, have a thermal coefficient of expansion approximating that of aluminum, and have the ability to withstand the curing temperature. The requirement that it be a solid insulator is a result of the method of connecting the electrodes, that of cleaving the ends and using silver epoxy, as shown in Fig. 48. One suitable material is a silicone and glass fiber laminate sheet which is manufactured by Dow Corning, has a thermal coefficient of expansion of $20\text{-}40 \times 10^{-6}/C$ and a distortion temperature of over 480°C. This material was used to make a twelve layer capacitor which was cured at 400 °C without developing bubbles. However the slight surface roughness of the laminate sheet caused the capacitors to be shorted. If a method could be developed for smoothing the surface this material would be suitable for use as a substrate.

The most successful capacitor fabricated was a nine layer device with a capacitance of 140,000pF and a dissipation factor of .0063. Several one layer capacitors were fabricated with dissipation factors as low as .004, which should be obtainable on multilayer capacitors once the substrate problem is rectified.

Experiments were conducted to elucidate the frequency and temperature dependence of the capacitance and dissipation factor, and the results are depicted in Fig. 50 and 51. In Fig. 50, the capacitance decreases with both increasing temperature and frequency. The decrease in capacitance with the increase in temperature is attributable to a

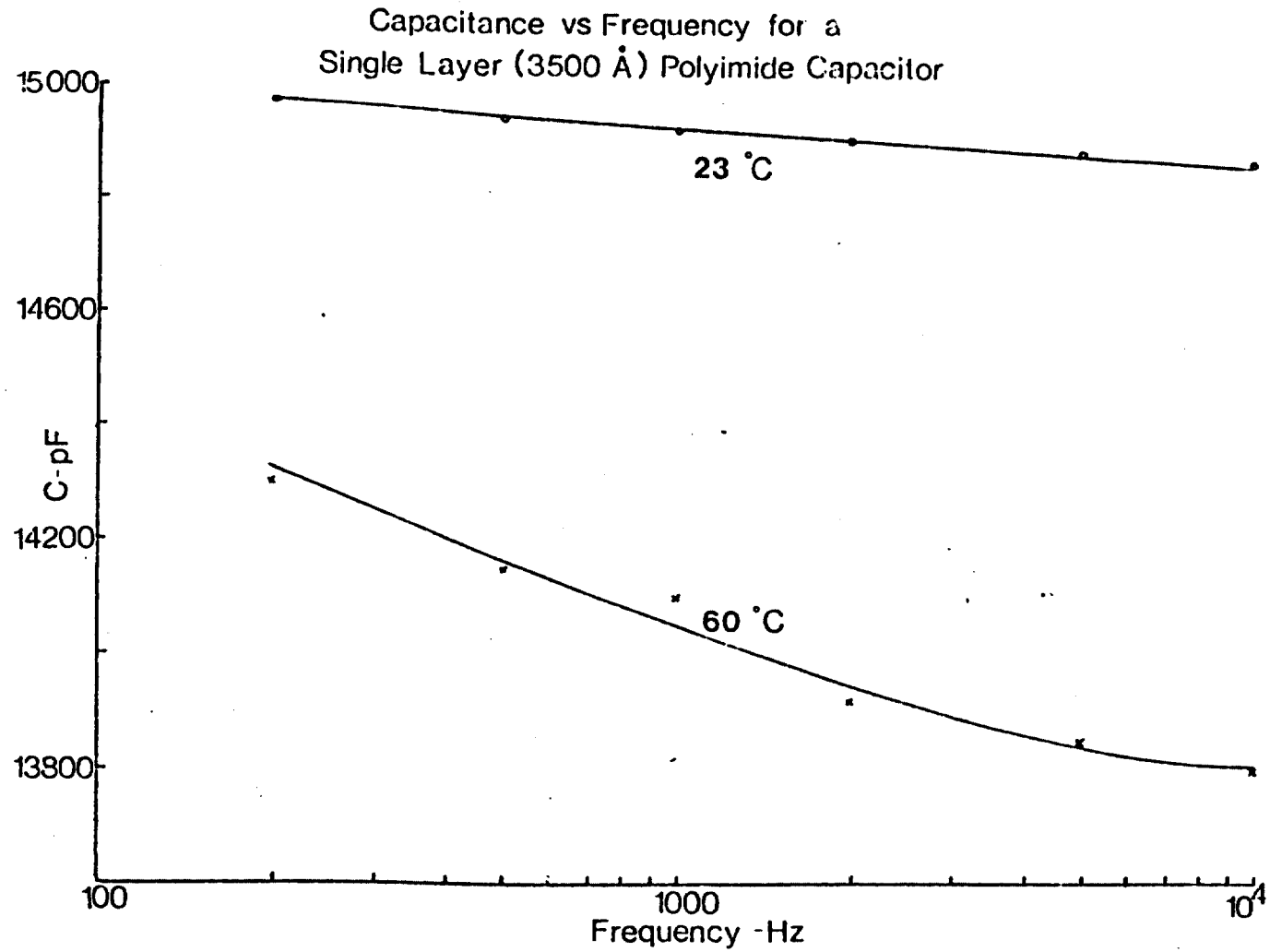


Figure 50. CAPACITANCE AS A FUNCTION OF FREQUENCY AND TEMPERATURE.

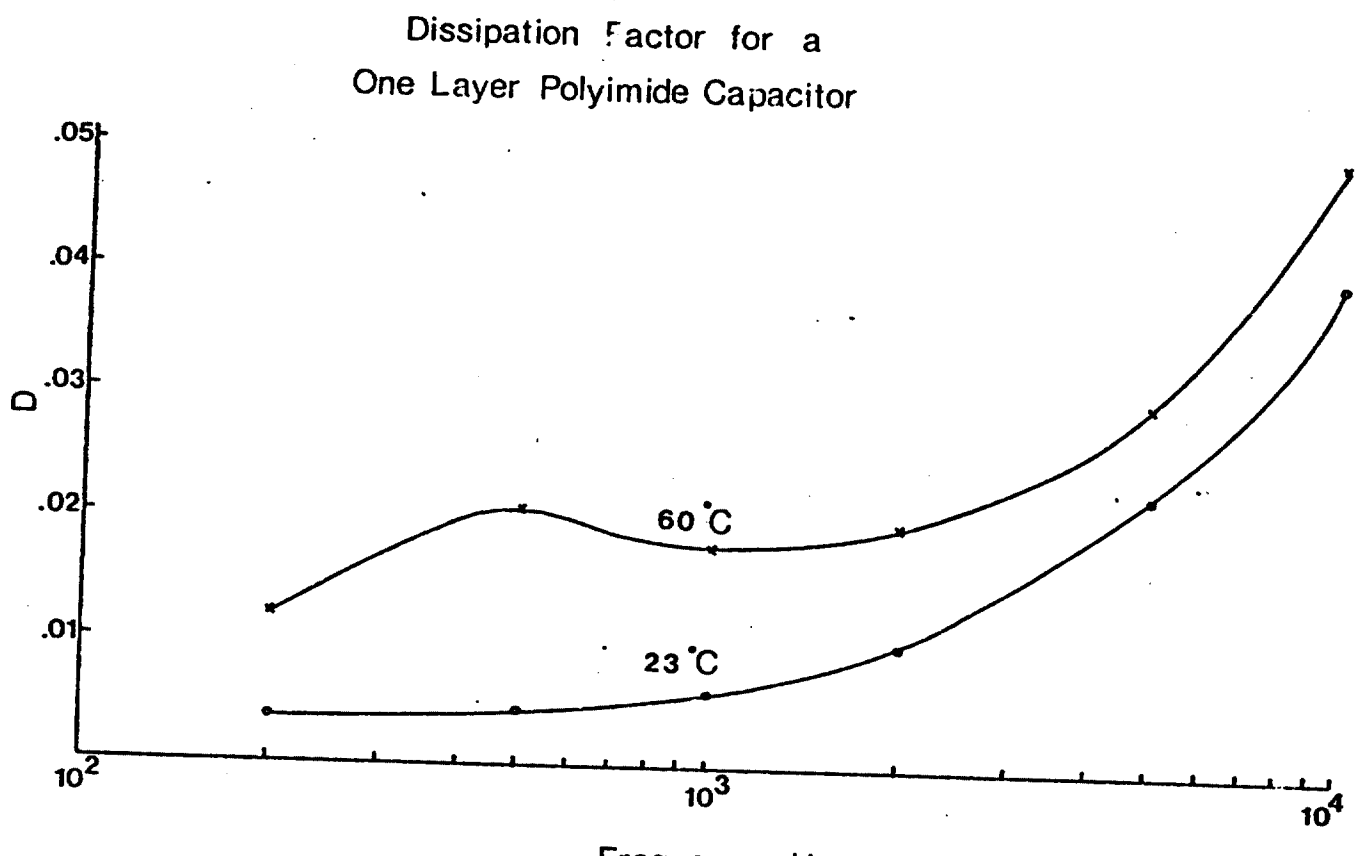


Figure 51. DISSIPATION FACTOR AS A FUNCTION OF FREQUENCY AND TEMPERATURE.

slight expansion of the dielectric material which overwhelms any contribution due to an increase in the dielectric constant. The decrease in capacitance with increasing frequency is attributable to a decrease in the dielectric constant, as is typical of nonpolar polymers. The increase in the dissipation factor with increasing frequency is a result of the increased contribution of the series resistance of the electrodes. The increase in the dissipation factor as a function of increased temperature is result of the resistivity of the dielectric decreasing as a function of temperature.

2.2 KODAK METAL ETCH RESIST

Kodak Metal Etch Resist (KMER) is a negative photoresist. The typical processing procedure for KMER was to spin for 30 seconds at the desired speed. The resist was baked for 30 minutes at 85°C. Exposure time was 30 seconds, followed by 30 seconds in KMER developer. The resist was rinsed for 30 seconds in Kodak microresist rinse and then hard baked at 185°C for 30 minutes.

Capacitance verses spin speed for undiluted KMER is shown in Fig. 52. Pure KMER tended to form cobweb like strands during the spin-on step, which frequently fell on top of the substrate. For this reason a dilution of two parts KMER to 1 part KMER thinner is now used. No changes were made in the process parameters, however the film thickness has decreased.

Capacitance and dissipation factor as a function of frequency and temperature are plotted in Figs. 53, 54 and 55. The results are typical for a single layer device on a glass substrate using undiluted KMER.

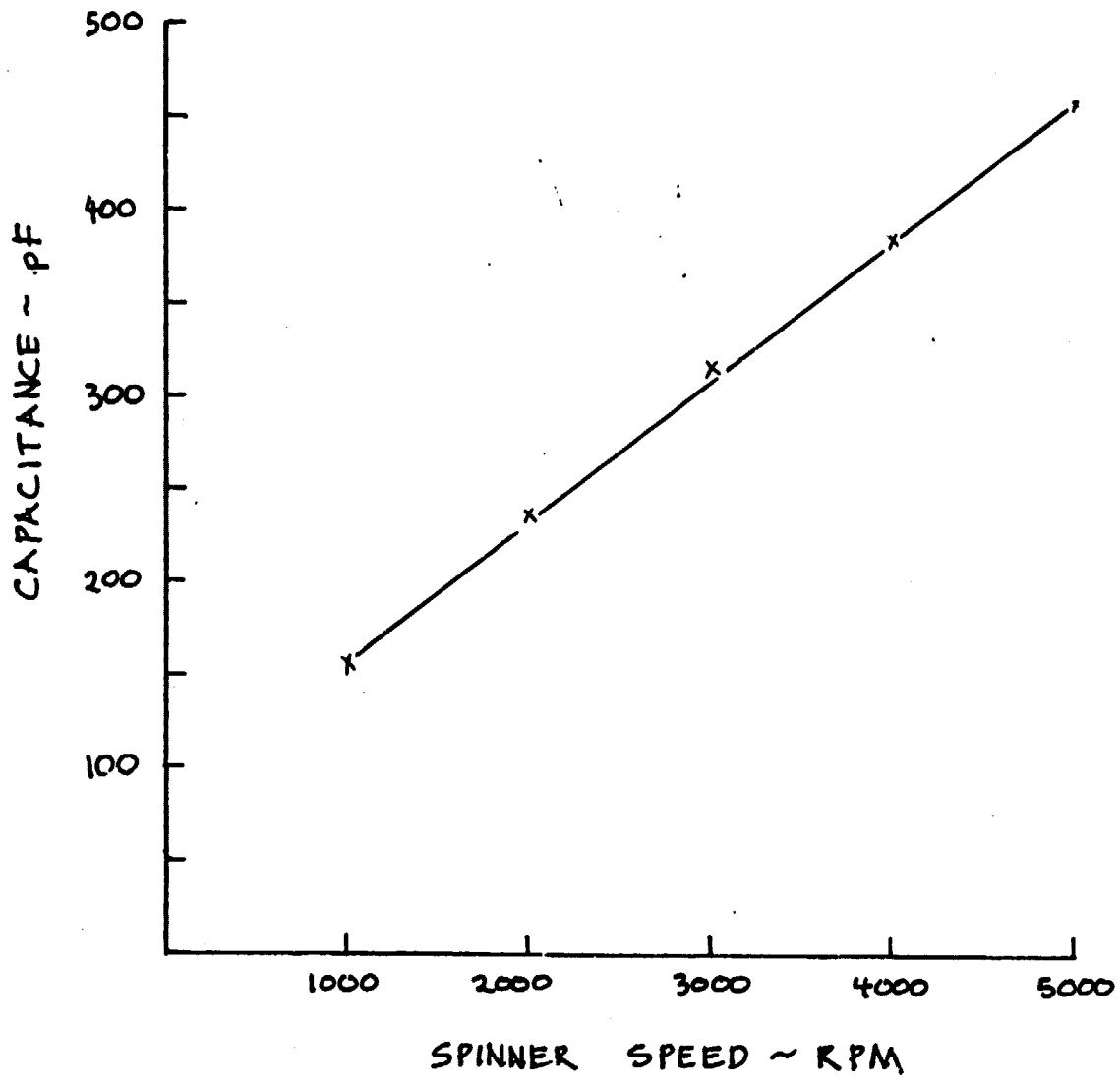


FIGURE 52 CAPACITANCE VS SPINNER SPEED FOR KMER PHOTORESIST

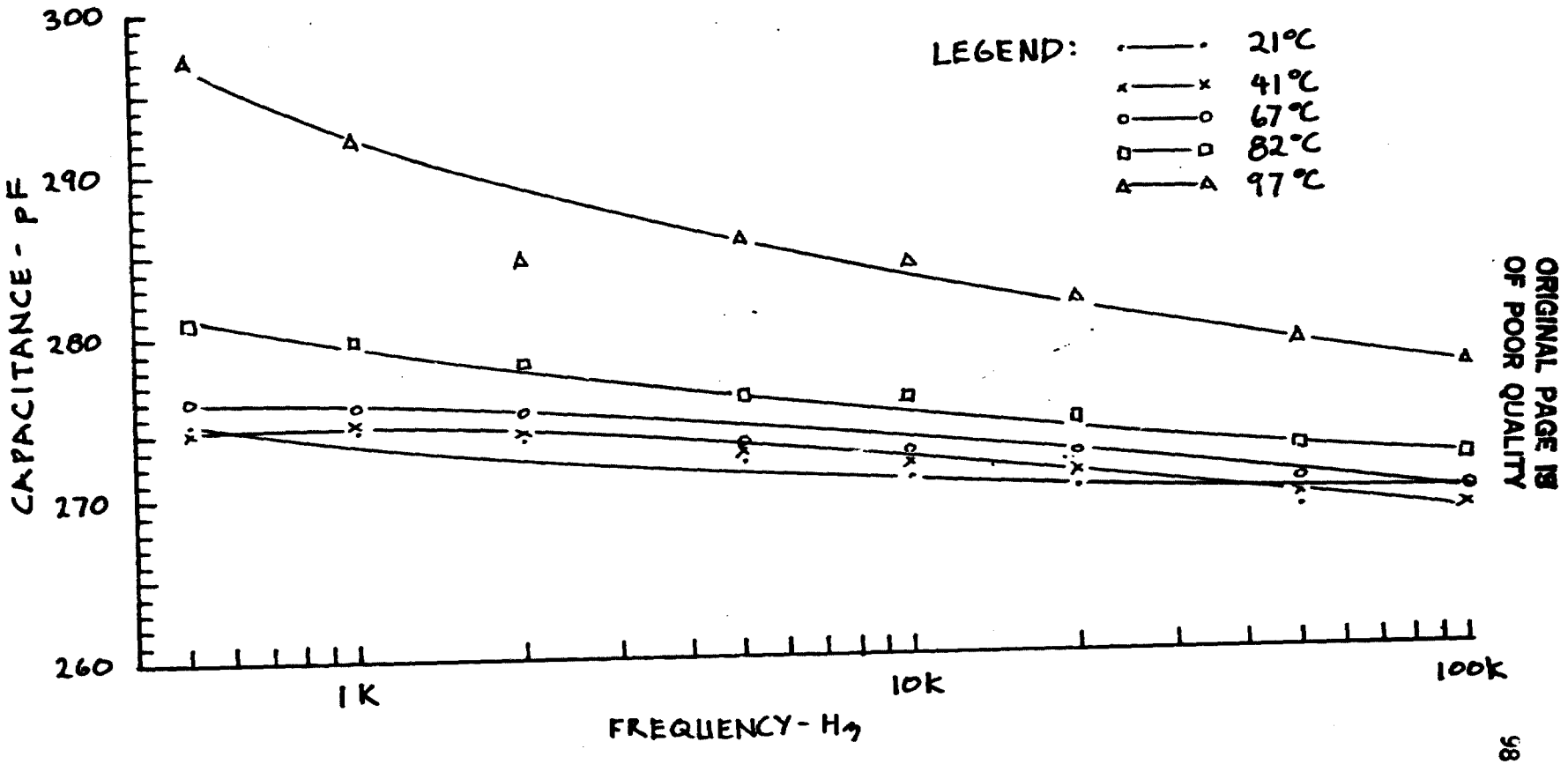


FIGURE 53 CAPACITANCE VS FREQUENCY FOR A SINGLE LAYER KMER CAPACITOR

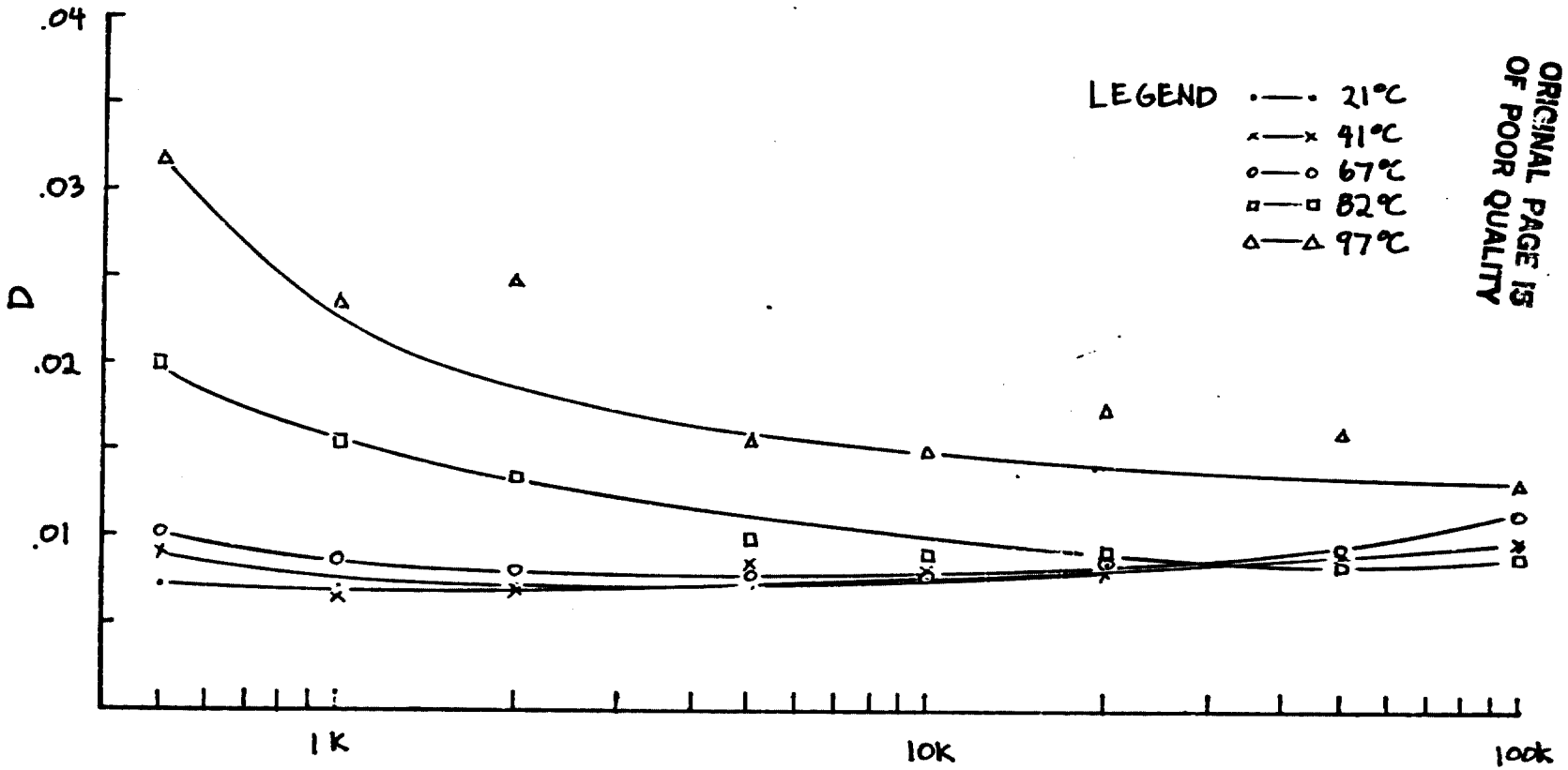
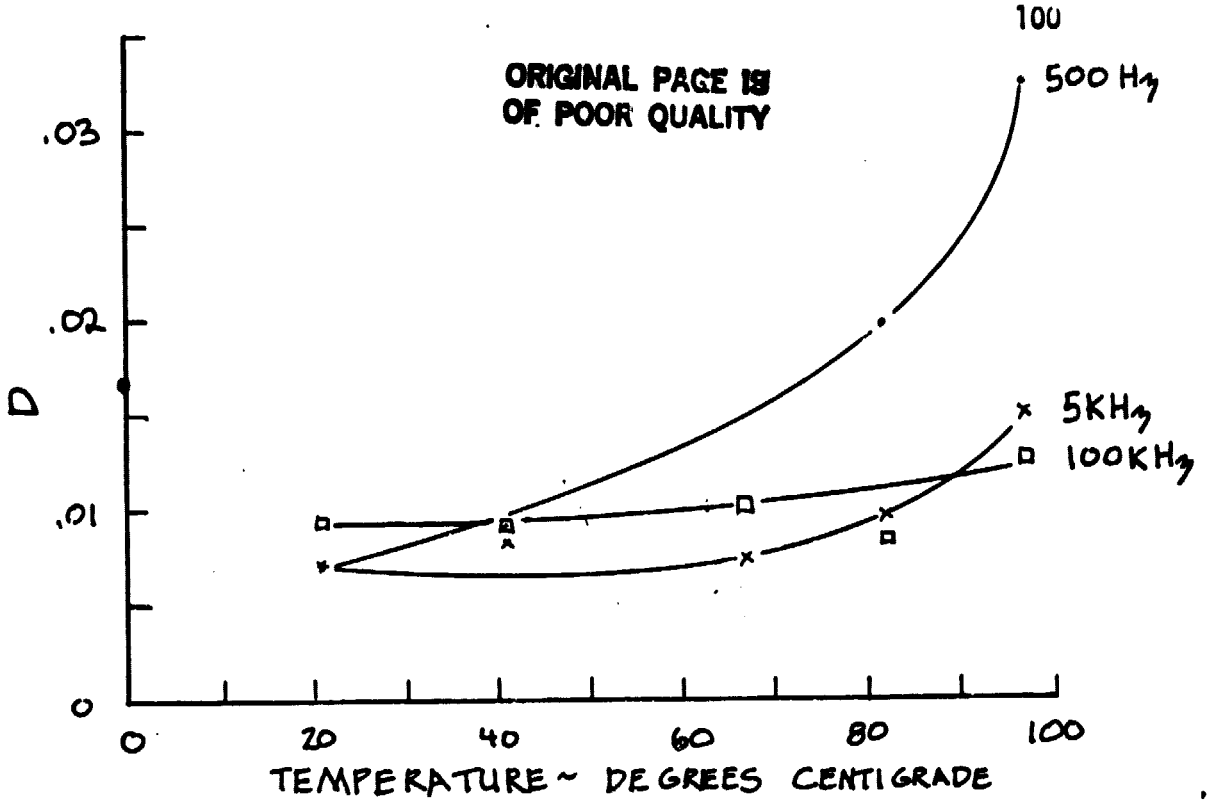


FIGURE 54 DISSIPATION FACTOR VS FREQUENCY FOR A SINGLE LAYER KMER CAPACITOR



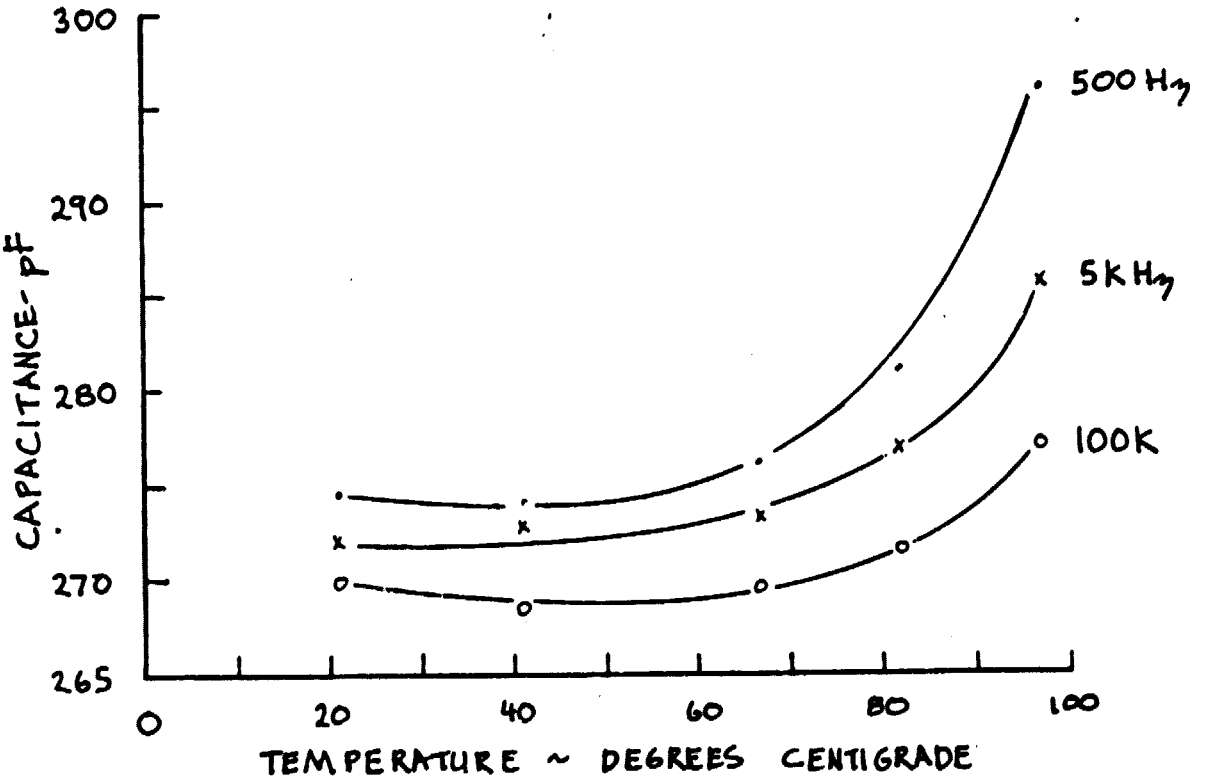


FIGURE 55 CAPACITANCE AND DISSIPATION FACTOR VS TEMPERATURE FOR A ONE LAYER KMER DEVICE

Multilayer devices have been constructed using the diluated KMER on glass and ferrotype substrates. Before device fabrication was started on the ferrotype substrate, it was coated with fully cured polyimide layers. Pyralin 2566 mixed with an equal amount of T-9035 thinner was spun on twice at 800 RPM for 30 seconds for each layer and then baked 30 minutes at 350°C. Single layers of pure KMER have also been applied to the ferrotype substrate with good results, but no multilayer devices have been made using pure KMER base layers.

The only problem in using KMER was a bubbling of the top metal layer. During the hard bake of the most recently applied KMER layer, the top-most layer of aluminum bubbled up, but no bubbles appeared elsewhere on the plate. This has occurred on all multilayer structures made on both the glass (HRP) and ferrotype substrates. The probable cause is that the hard bake is not sufficient to expel all of the solvents in the photoresist. After a metal layer was deposited and the device was heated up in the next hard bake cycle, the remaining solvents were trapped under the aluminum film and could not escape, causing it to bubble. Efforts to completely drive out solvents during the hard bake have had modest success.

By using a two hour hard bake at 185°C a two layer device was made. Only a one layer device could be made with the original 30 minute hard bake. A 30 minute, 185°C bake in a vacuum oven, followed by a 30 minute bake at 250°C on a hot plate produced up to three layer devices. In both cases the top metal layer always bubbled. More work is needed to find a satisfactory hard bake.

2.3 MICRORESIST 747

Microresist 747 is a negative photoresist manufactured by Kodak. It is filtered by the manufacturer to an absolute value of 0.5 micrometers and is applied unfiltered and undiluted, directly to the substrate. The plate was spun for 30 seconds at 2000 RPM and soft baked 30 minutes at 85°C. Exposure time was three seconds. The photoresist was developed one minute in Kodak microresist developer and rinsed in Kodak microresist thinner for 30 seconds. A 30 minute, 125°C hard bake was the final step.

A device with a maximum of two layers could be made using the above process. By applying two layers of photoresist, a working six layer device was fabricated. A short 10 minute soft bake was performed between the two layers of photoresist. All other processing steps remained the same, except the exposure time was increased to five seconds. The dual layer increased the film thickness and greatly reduced pinholes. The dissipation factor was quite high after three or four layers had been fabricated. This was thought to be caused by small defects that could be removed by discharging a capacitor through the device. This was done on the six layer device after each new metal layer was deposited on half of the devices. The dissipation factor was noted to be about an order of magnitude lower and the yield increased for devices subjected to the electrical discharge.

Metal was removed from the localized defects during the discharge and, if the current was large enough, several self propagating defects resulted. Also, the edges of the metal at these sites may be several micrometers thick, leading to even more local defects in the next layer.

Capacitance as a function of spinner speed is shown in Fig. 56. Capacitance and dissipation factor as a function of frequency and temperature are given in Figs. 57, 58, and 59. All data is for a single layer capacitance using 747 with a viscosity of 110 centistokes and an area of 0.225 cm^2.

2.4 AZ-1350J

AZ-1350J is a positive type photoresist manufactured by The Shipley Company. All capacitor structures were made on PFO glass plates from Kodak with the emulsion removed. The photoresist was soft baked for 30 minutes at 95 °C after a 30 second spin-on application. Exposure and developing time were both 30 seconds. AZ-351 developer was used as the developer and the five minute rinse was done using deionized water. The hard bake was for 30 minutes at 125°C.

The best capacitor made was a three layer device with an average capacitance of 5400pF, indicating an individual layer thickness of about 0.4 micrometers. The spin speed was 3000 RPM. The first layer was very smooth but additional layers showed a build-up of photoresist near the edges of the metal stripes. This build up eventually caused shorts between the two pairs of electrodes and step coverage problems for the aluminum evaporation leading to opens or breaks in the metal stripes.

Another problem, common to all positive photoresist, was that they unpolymerized when exposed to light, even after the hard bake. For this reason, all processing steps must be performed in areas equipped with red or yellow lamps. Single layers of AZ-1350J, which had undergone full hard bakes, would completely decompose when left in ordinary room

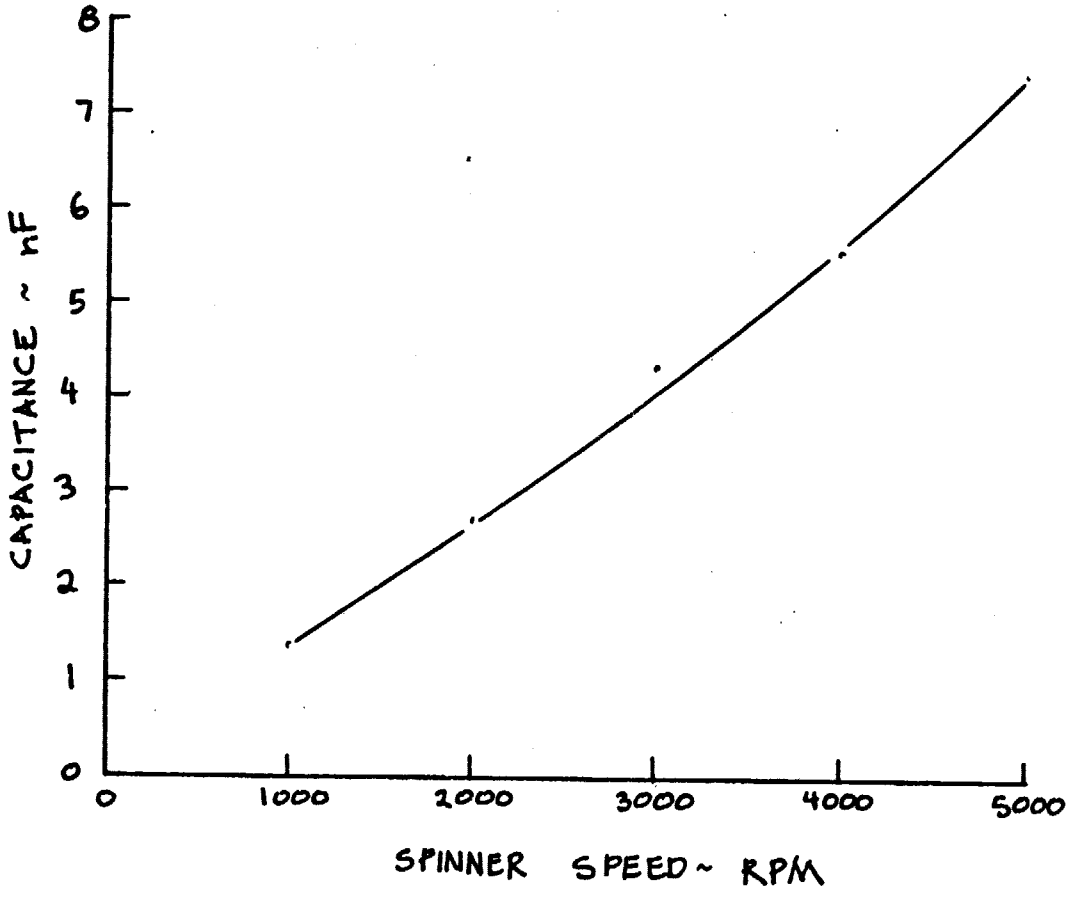


FIGURE 56 CAPACITANCE VS. SPINNER SPEED FOR KODAK MICROREGIST 747

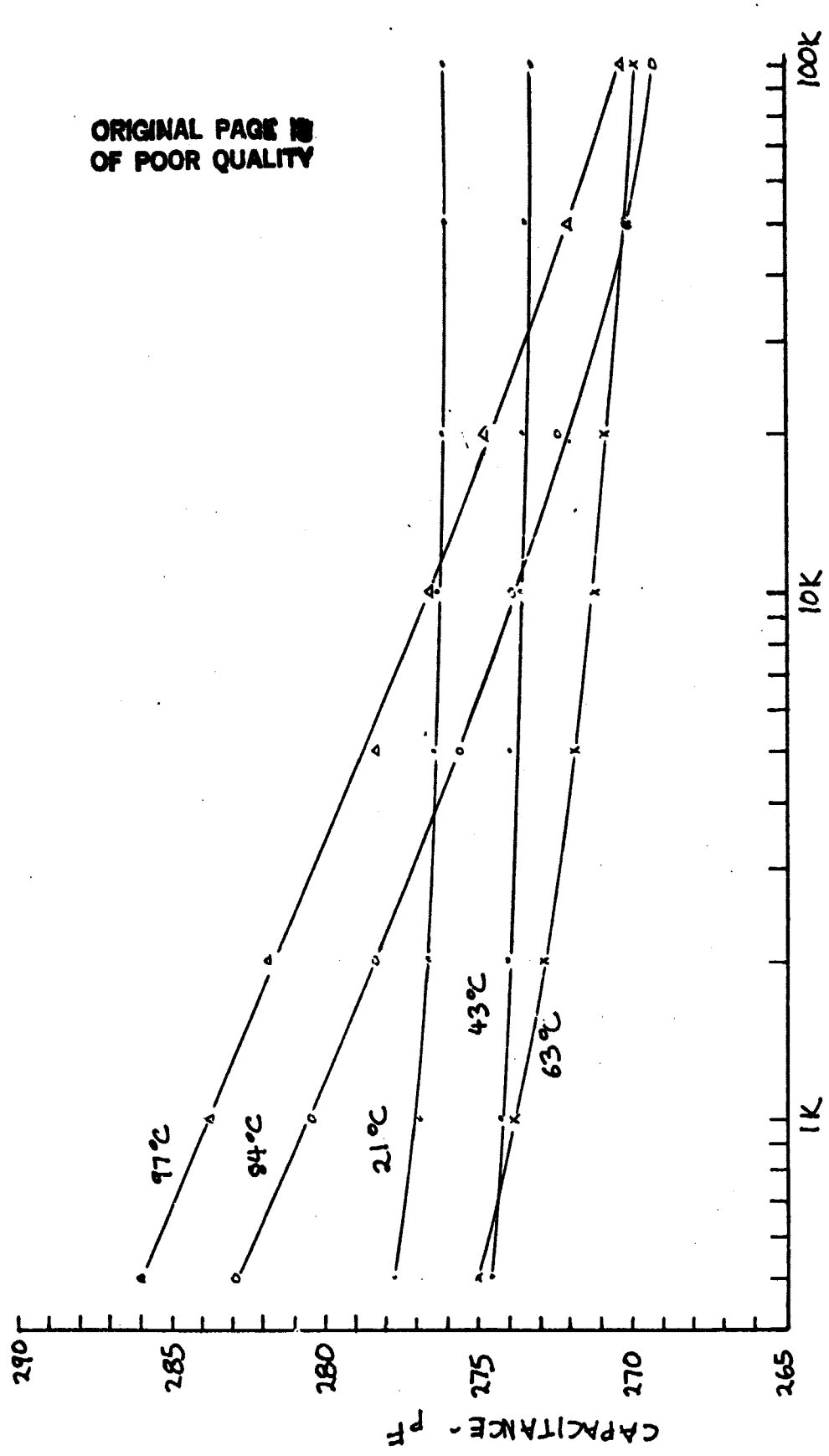


FIGURE 57 CAPACITANCE FOR A SINGLE LAYER 747 CAPACITOR

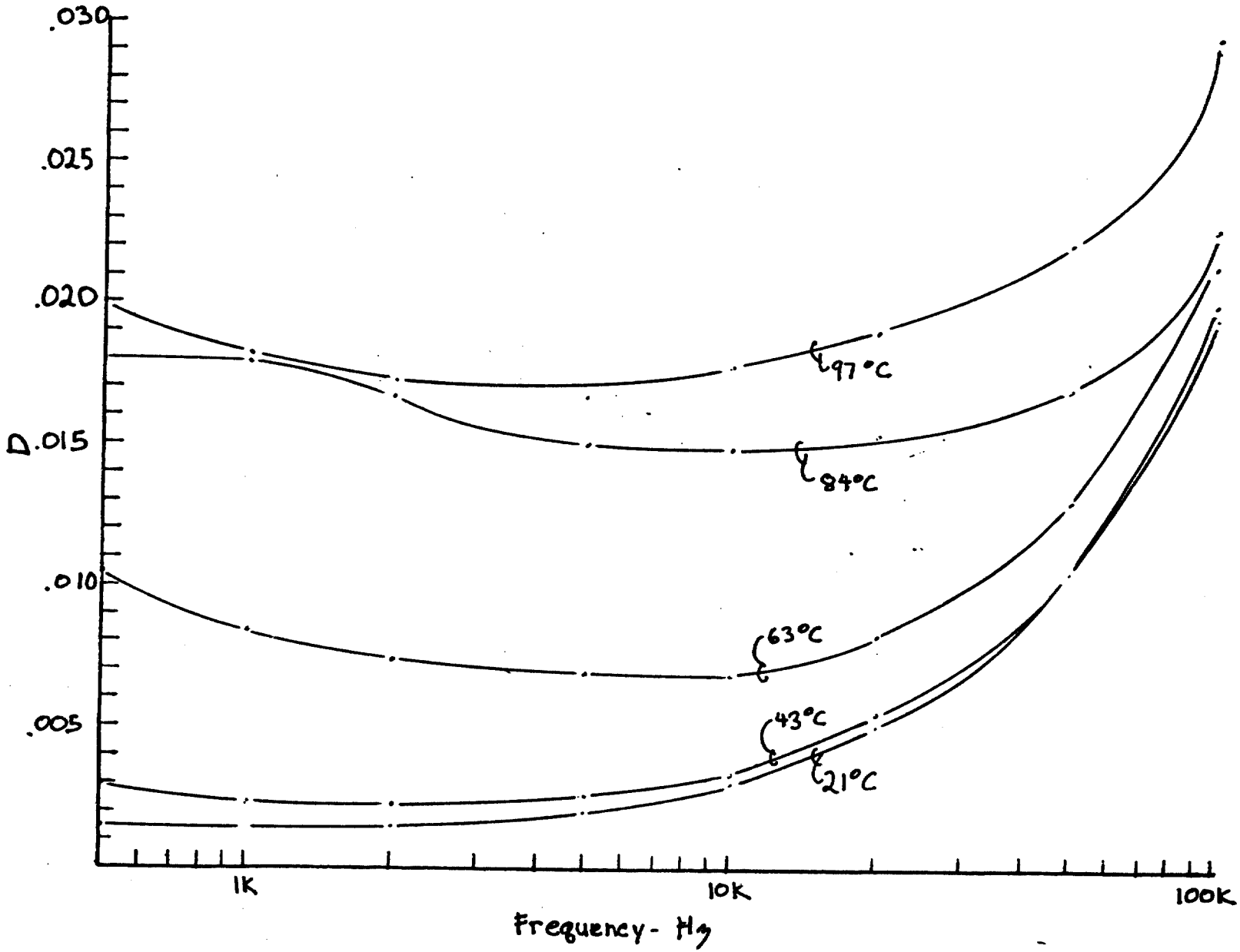
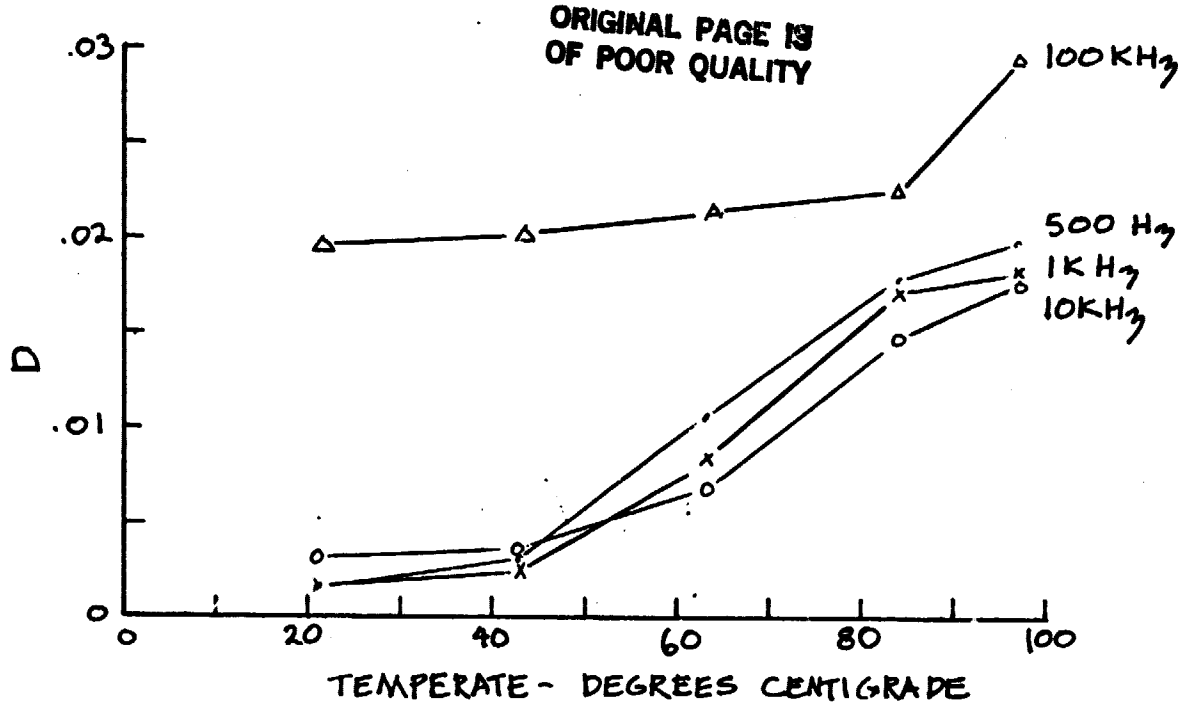


FIGURE 58 DISSIPATION FACTOR FOR A ONE LAYER 747 CAPACITOR



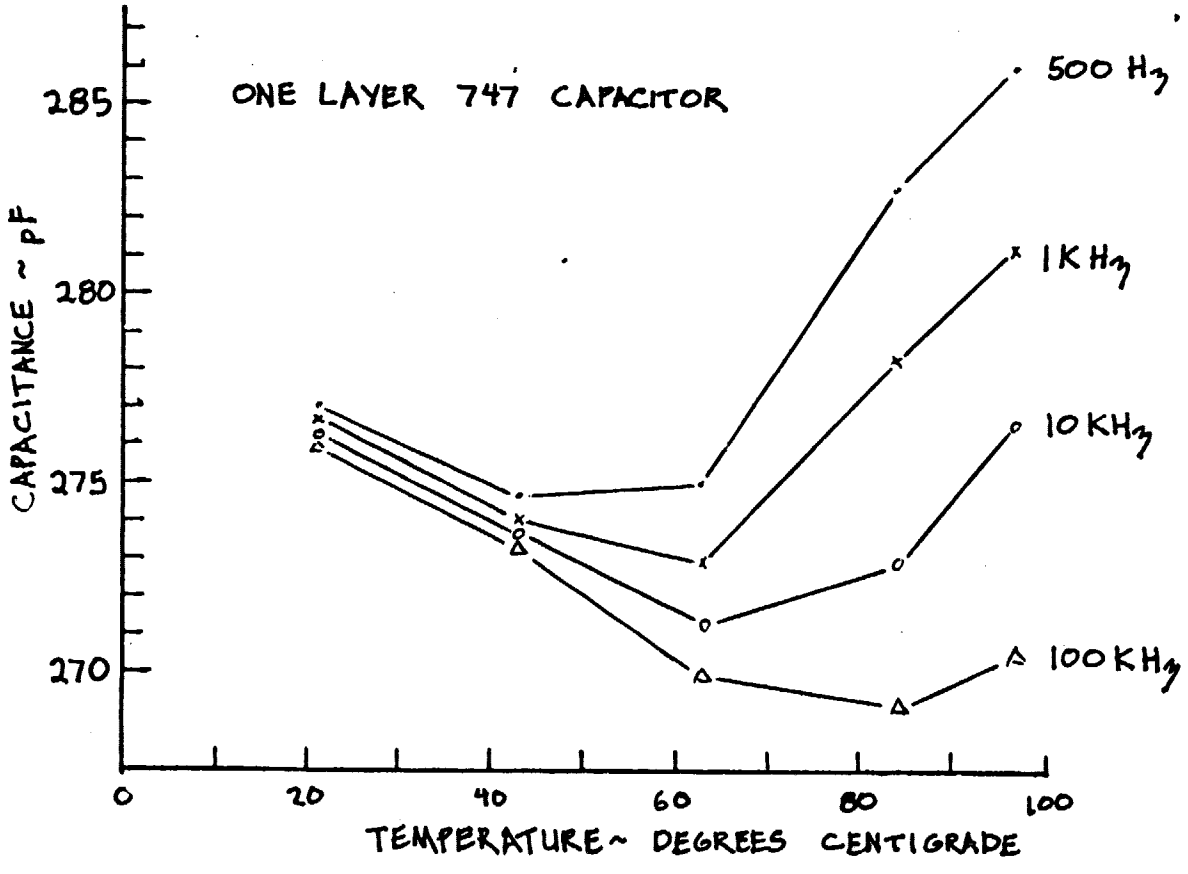


FIGURE 59 CAPACITANCE AND DISSIPATION FACTOR VS. TEMPERATURE

light for a few days. Yellow lamps were installed in the evaporation room and rubylith, a red mylar film, was placed over the lamps and glass front of the fumehood to provide a safe area for testing.

Capacitance as a function of spin speed is shown Fig. 60. Capacitance and dissipation factor as a function of frequency and temperature is given in Figs. 61 and 62 for single layer devices with an area of 0.225 cm^2 and a spinner speed of 3000 RPM.

2.5 Defect Studies of Polymers

2.5.1 Pinhole Decoration

To help visualize cracks, pinholes and other defects in thin, insulating films a reverse carbon decoration procedure was implemented. The desired dielectric material was processed normally on a conducting substrate. If the substrate was not conductive, a thin aluminum evaporation on the substrate surface with a wire attached using silver epoxy was sufficient for making contact to the ground plane. The sample was placed on a ground plane with a wire grid two centimeters above. The entire setup was in an enclosed box with dry air flowing to keep the relative humidity as low as possible. A 5,000 to 10,000 volt D.C. bias was applied to the grid, for 30 sec., setting up an electric field. Nitrogen was attracted to the surface of the dielectric and remained there fore a short length of time after the bias field was removed. The plate was then dipped into a solution containing carbon black particles for 10 seconds. Carbon was deposited where charge had accumulated on the surface of the dielectric. Where pinholes and cracks exposed the ground plane, no carbon was deposited. The contrast between regions

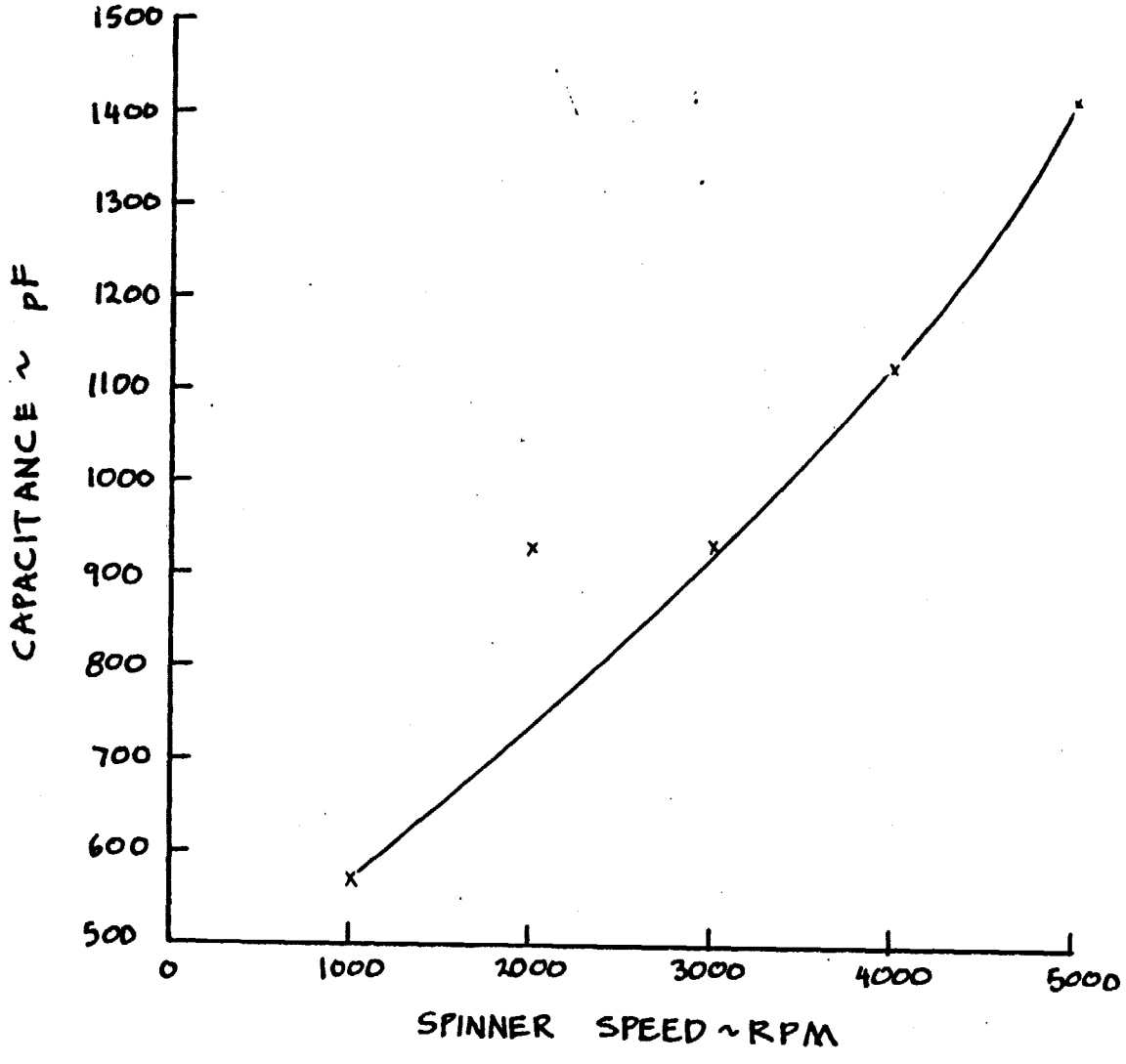


FIGURE 60 CAPACITANCE VS SPINNER SPEED FOR SHIPLEY AZ-1350J

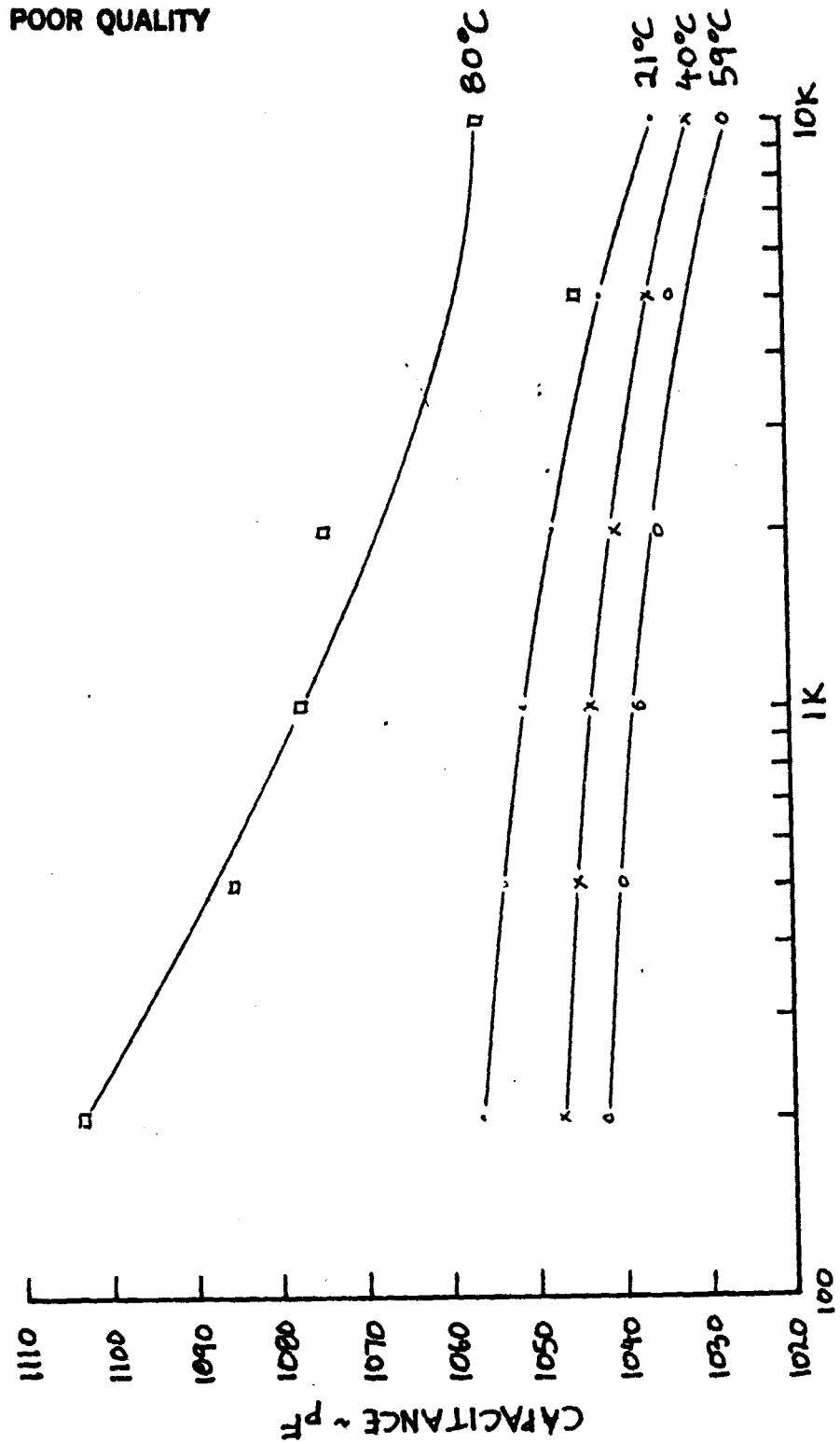


FIGURE 61 CAPACITANCE VS FREQUENCY FOR A SINGLE LAYER DEVICE MADE WITH SHIPLEY A2-1350J

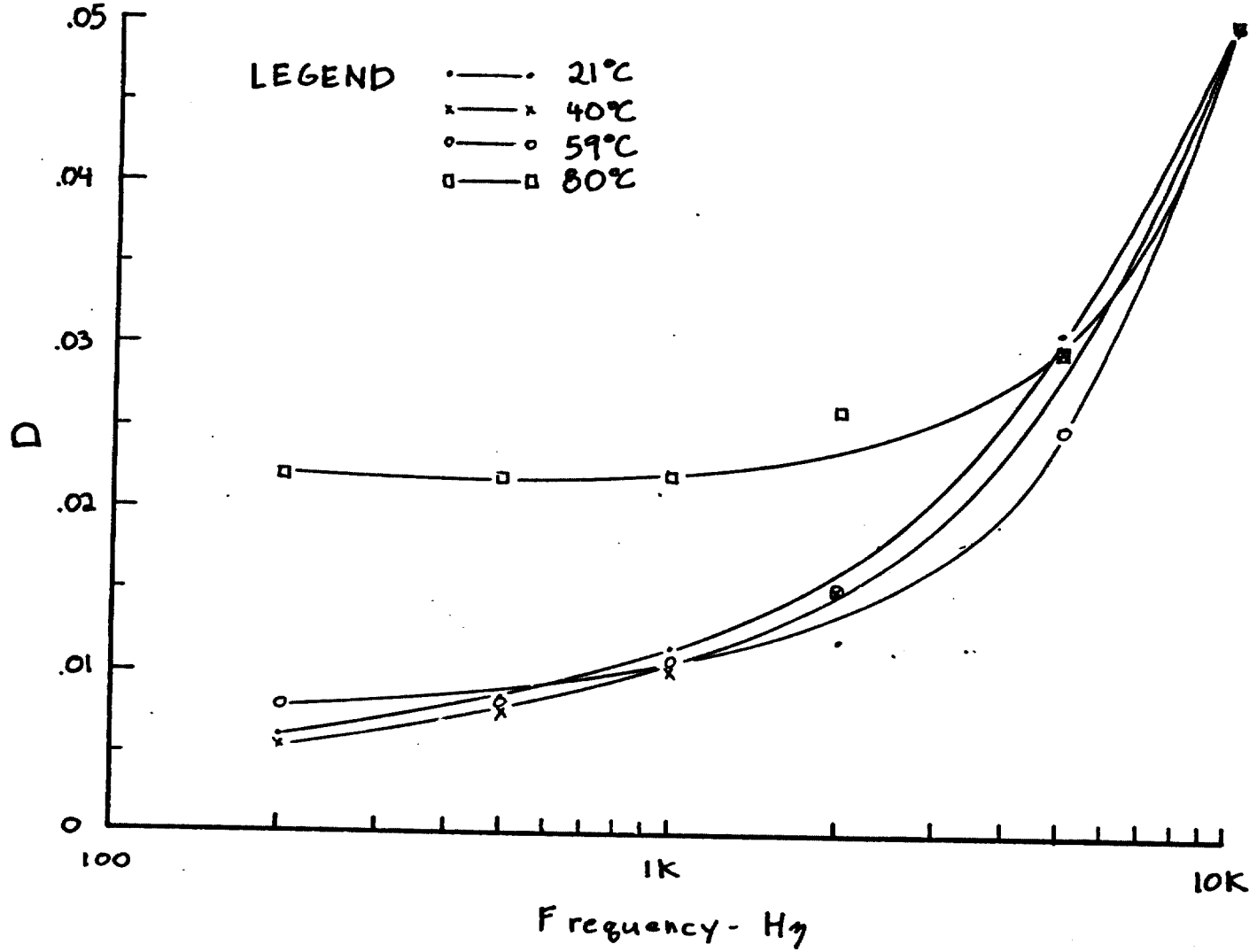


FIGURE 62 DISSIPATION FACTOR VS FREQUENCY FOR A SINGLE LAYER DEVICE MADE WITH SHIPLEY AZ-1350J

with and without carbon deposition was readily visible and features in the range of 0.1 mil were visible under microscopic examination. Figure 63 is a graphic depiction of this setup. Figure 64 is a photomicrograph of a polyimide layer, depiciting typical results obtainable with this method.

The following table lists the substances and their concentrations that are used in the carbon decoration procedure. The concentrated solution was mixed ultrasonically for 1 hour before adding it to the $C_2Cl_3F_3$ to form the working solution.

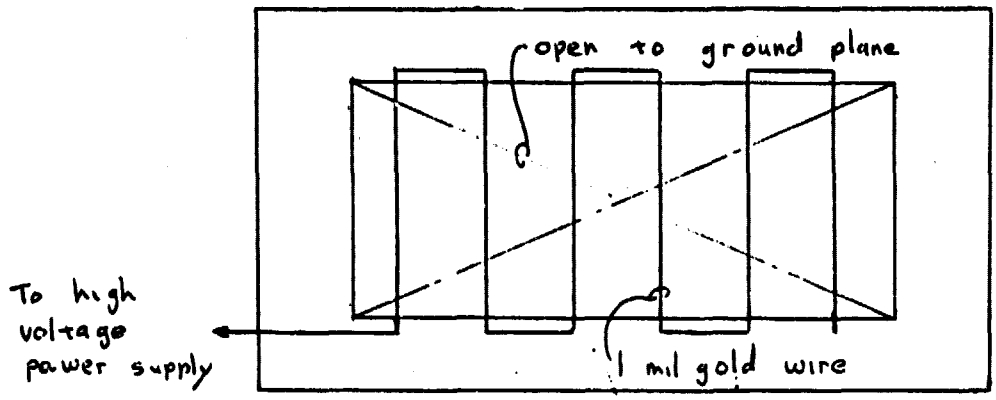
CONCENTRATE:		
	Carbon Black, 2000A diameter	17 gm
	Toluene	100 ml
	50gm/50ml of Lubrizol 894/toluene	10 ml
	50gm/90ml of AC 430 copolymer/toluene	10 ml
WORKING SOLUTION:	CONCENTRATE	2-5 grams
	$C_2Cl_3F_3$(FREON 113)	400 ml

Table VI: Solutions for carbon decoration process

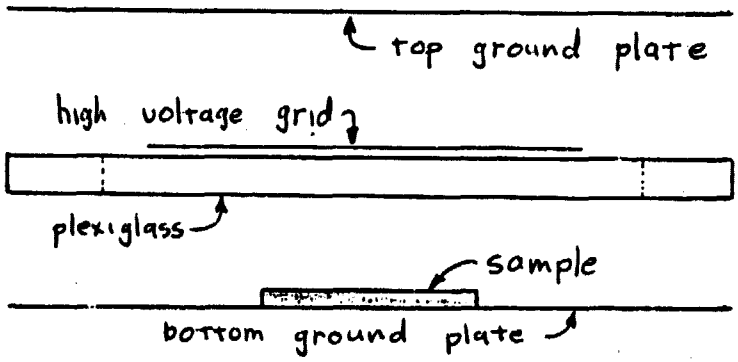
As seen in Fig. 64, there are several small white areas that are not covered with carbon. It is difficult, even under high magnification, to see if pinholes are actually present at these sites. This makes it very difficult to determine pinhole density with confidence, but the method does give a good indication of overall film quality.

2.5.2 Breakdown Voltage Studies

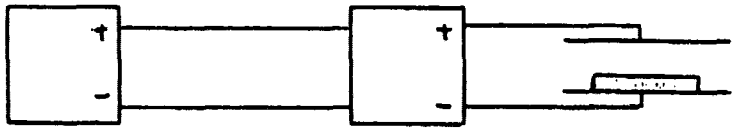
In some of the capacitors, we noted that possibly due to structure defects or ionic contamination in the dielectric that the breakdown



TOP VIEW: HIGH VOLTAGE GRID



BOTTOM VIEW



SCHEMATIC DIAGRAM

FIGURE 63 REVERSE CARBON DECORATION EQUIPMENT

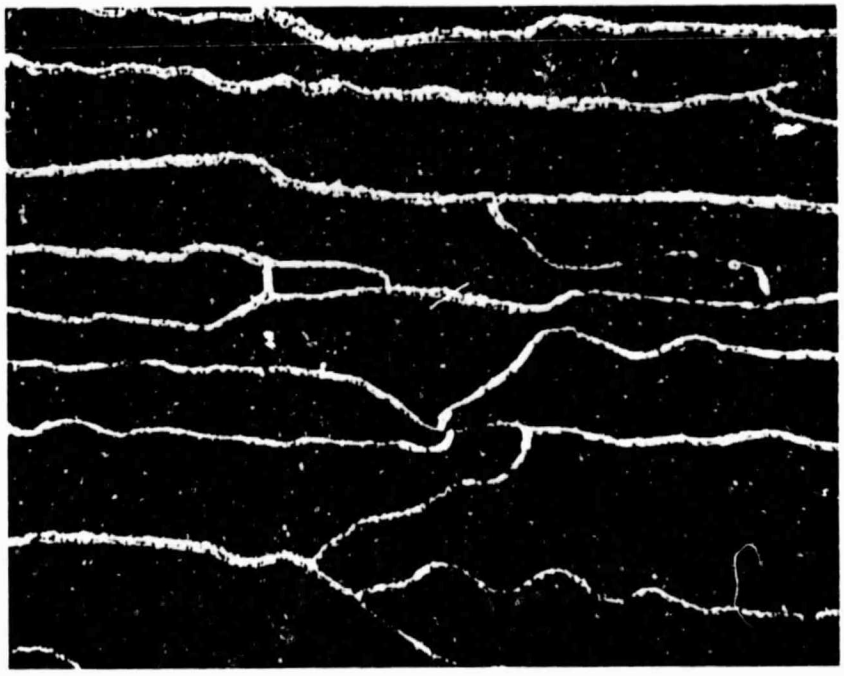


FIGURE 64 PHOTOMICROGRAPH OF AN ALUMINUM SUBSTRATE WITH A SINGLE LAYER OF PYRALIN 2555 POLYIMIDE. REVERSE CARBON DECORATION HIGHLIGHTS CRACKS IN THE POLYIMIDE. (50 x MAGNIFICATION)

voltages seemed to be rather low in relationship to that which was expected from dielectric strength information supplied by the manufacturer. To better understand the nature of these breakdowns, a special experiment was run, the block diagram of which is shown in Fig. 65. Figure 66 shows some of the electronic circuit details of a system that counts self healing defects. When a dielectric film is stressed with a sufficient voltage, a large current will flow through a localized defect and heat it. If the top electrode is made thin enough, in the range of 1500 angstroms or less, the metal and defect are destroyed by the joule heating. After the defect is removed, the current is reduced to the normal charging current. This temporary increase in current is detected and recorded on an event counter.

The data may be plotted as events versus applied voltage, or vs. electric field if the film thickness is known. The effects of specific process parameters on dielectric breakdown and, therefore, film quality, can be determined fairly easily. Important factors to consider in comparing results are final breakdown voltage, relative spread of events over voltage and the total number of events.

Figure 67 shows a plot typical of this process for a capacitor using KODAK microresist 747 as the dielectric material and aluminum electrodes. No obvious grouping of the data into primary, secondary and tertiary regions can be discerned from this data. Aluminum is known to form hillocks readily and this was initially thought to be the cause of the almost continuous spread of events in Fig. 67, since variation of hillock height across the capacitor could produce this kind of result.

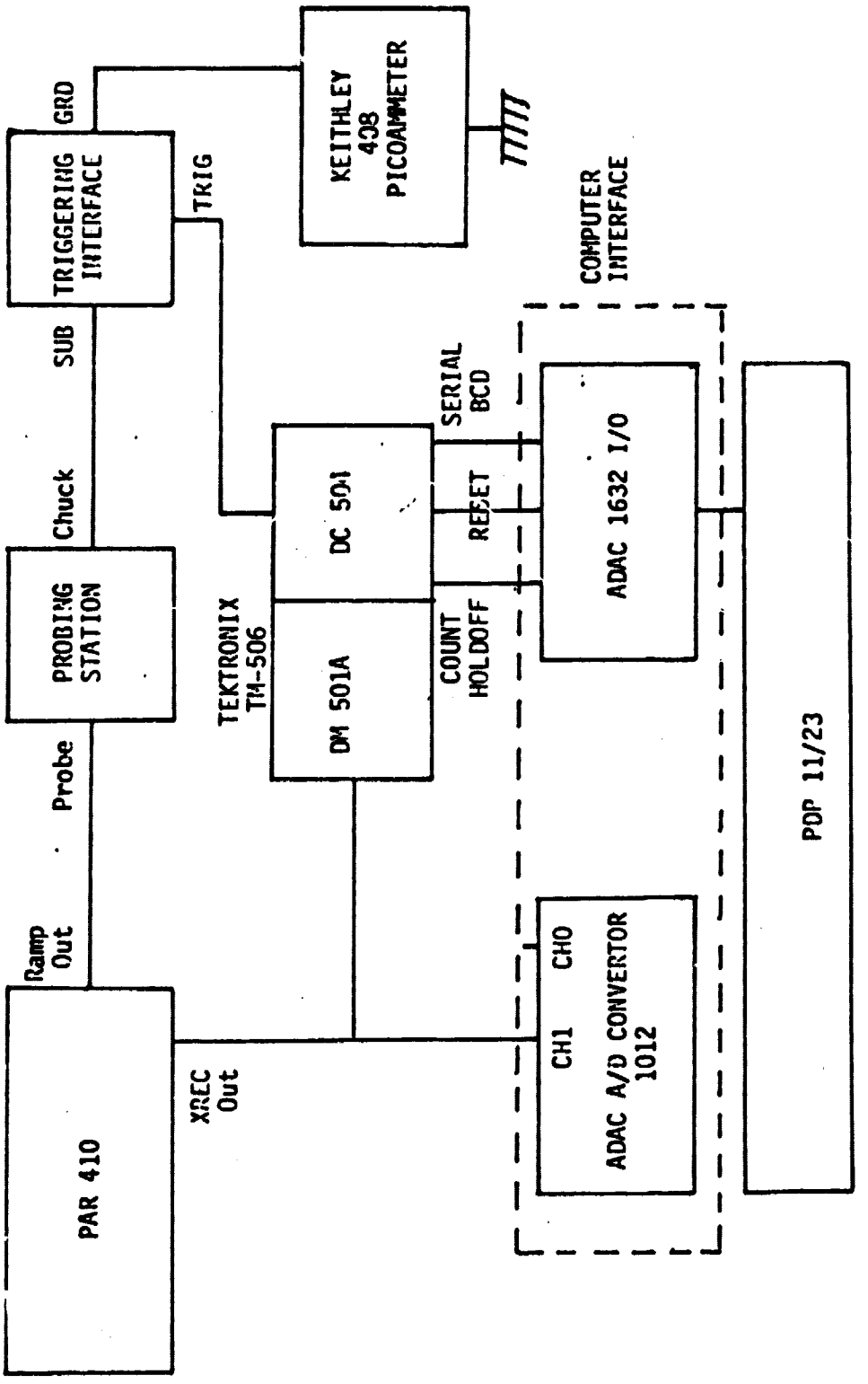


Fig. 65 Functional block diagram of the measurement system.

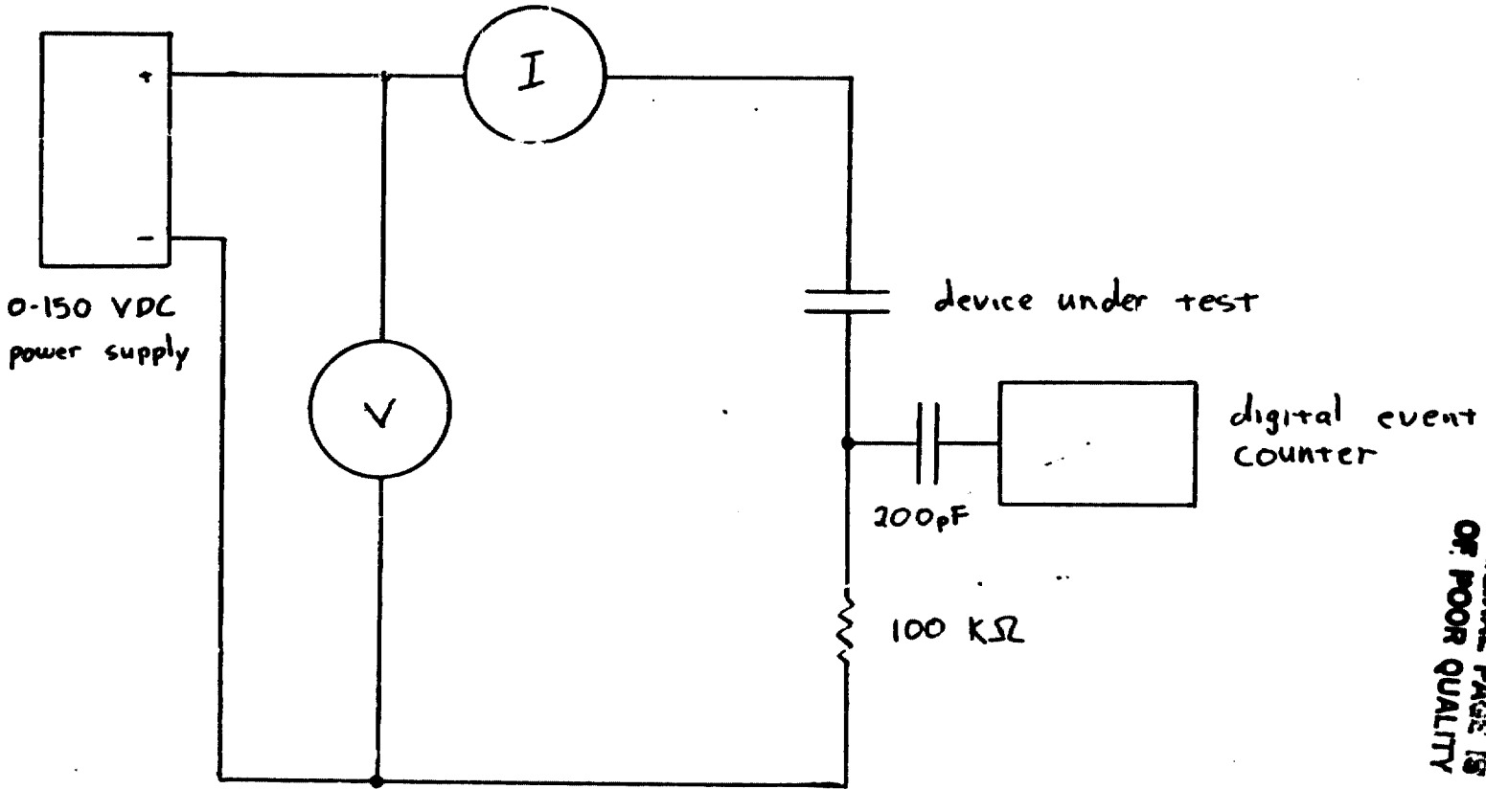


FIGURE 66 SELF HEALING BREAKDOWN EVENT COUNTER

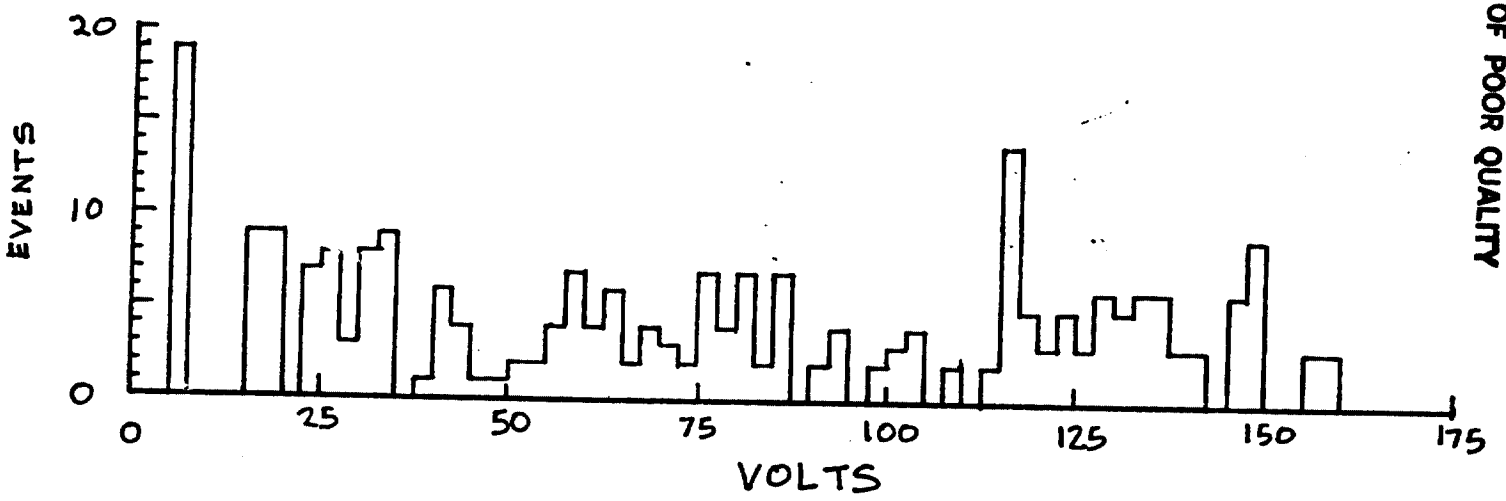


FIGURE 67 SELF HEALING BREAKDOWN EVENTS VS VOLTAGE FOR A ONE LAYER 747 CAPACITOR

Several variations on the metallization procedure were tried and analyzed, keeping processing steps for the 747 the same. All the variations produced the same results indicating that either the hillocks are not the cause of the majority of breakdown events or that the changes made in the metallization procedure did not significantly change the surface features of the resulting film.

When taking current readings the electrometer varied wildly in the breakdown range. If the ramp was held constant the current sometimes stablized indicating that the breakdowns had quit. When this happened one found that these currents were reproducible and ohmic. It was felt the polyimide on minor breakdown created a carbon streak connecting the electrodes. These carbon streaks did not create excessively large currents but did give an ohmic response that is seen at lower voltages indicating that possibly the sample has some small carbon streaks in it before a voltage was applied. This was so, since after allowing a sample to have a large voltage across it for 30 minutes, most of the aluminum electrodes was literally blown away and the polyimide was black in color indicating it had experienced heavy joule heating and, yet the sample produced an ohmic response later at lower voltages.

All of this still did not tell us why these carbon streaks were occurring. Inadvertently it was noticed that when applying the silver epoxy to the sample after scribing that long thin strands of the epoxy were repelled by the sample. This could be static charge picked up somewhere in the processing. This has not been proven as the culprit for early breakdowns but is one possibility.

2.5.3 Conduction Mechanism Studies

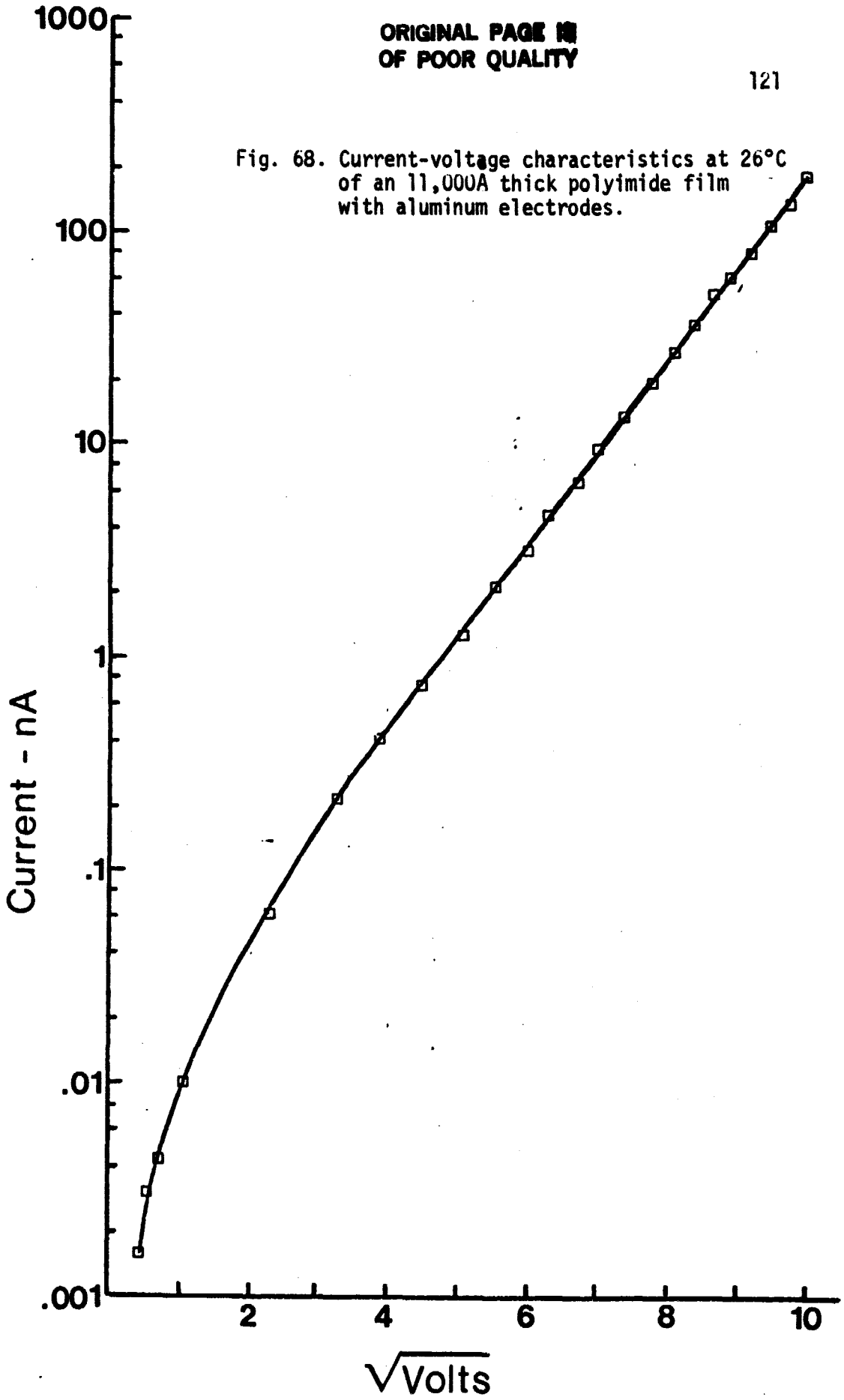
Part of the dissipation factor in a dielectric is related to the conduction through the material. Because some of the dissipation factors measured in polyimide were somewhat higher than desired, it was decided to explore more carefully some of the underlying reasons for conduction in polyimide.

We concentrated mainly on films of from 4000A to 11,000A in thickness. Studies were made with aluminum electrodes and the conduction mechanisms were deduced from graphs of the current as a function of voltage and temperature.

In order to aovid electromagnetic interference during the current-voltage measurements, the entire measurement setup was enclosed in a shielded cage. The currents were measured using a Keithley 610°C electrometer in series with the structure and the voltage was measured across the entire circuit with a Data Tech 350 digital multimeter. The voltage readings were corrected for the voltage drop across the electrometer.

The typical curve of current-voltage characteristics is shown in Fig. 68. The almost perfect straight line fit to the ln I versus $V^{1/2}$ plot seems strongly to suggest either a Schottky mechanism or a Poole-Frenkel mechanism, both of which are electronic processes as opposed to ionic. There is, however, the possibility of being misled by such a plot. There are regions of the curve of a hyperbolic sine function which when plotted on the same graph would also show roughly a straight line. If that were the case, then the conduction mechanism might be due

Fig. 68. Current-voltage characteristics at 26°C of an 11,000A thick polyimide film with aluminum electrodes.



to ions and described by the rate theory. This possibility was eliminated for the curve shown by carefully plotting several hyperbolic sine functions in an attempt to force a fit over the range plotted. There were no parameters which could be adjusted to cause a reasonable fit over this range of current and voltage.

Thus it seems clear that at room temperature and low fields that the conduction process is electronic in nature. The equations governing the current-voltage relationships for Schottky and Poole-Frenkel effects are:

$$J = A_R T^2 \exp(-\phi_S/kT) \exp(\beta_S E^{1/2} kT) \text{(Schottky)} \quad (1)$$

$$J = A_R T^2 \exp(-\phi_{PF}/kT) \exp(\beta_{PF} E^{1/2}/kT) \text{(Poole-Frenkel)} \quad (2)$$

where

$$\beta_S = (q^3/4\epsilon_0\epsilon_r d)^{1/2} = \beta_{PF}/2$$

in which ϕ_S is the barrier height of the aluminum-polymide interface, ϕ_{PF} is the depth of the trap level, A_R is Richardson's constant, T is absolute temperature, q is the electronic charge, k is Boltzmann's constant, ϵ_0 the permittivity, ϵ_r the dielectric constant and d is the polymer thickness. In order to distinguish between the two mechanisms it is only necessary to determine the slope of the ln I versus $V^{1/2}$ curve since the slope for the Poole-Frenkel effect is twice that of the Schottky effect. When that is done, however, it turns out that the experimental β is: $\beta_{exp} = 1.36\ \beta_S$ which puts the results in between that of the two effects.

It is not at all unreasonable to assume that both effects are present, the Schottky effect being controlled by the electrode-polymer

interface characteristics and the Poole-Frenkel effect being controlled by the bulk polymer characteristics. In any case, it seems clear that the room temperature conduction is electronic in nature.

A plot of the conductivity as a function of temperature is shown in Fig. 69. The electronic type of conduction was measured at room temperature where the slope of the curve shows an activation energy of 0.36 eV which is typical of impurity conduction mechanisms. At about 60°C there is a sharp increase in the conductivity activation energy to a value of 1.04 eV. Because cured polyimide does have an affinity for water absorption and because the samples were stored in a relatively high humidity (70%) environment, it is quite probable that this conductivity range from 60 °C to about 100 °C corresponds to the dissociation of loosely bound water molecules.

If this does indeed correspond to ionic conduction, then the current-voltage characteristics should change at higher temperatures for the $I \alpha \exp(V^{1/2})$ curve to a curve in which the current-voltage characteristic is described by the rate theory:

$$I = I_0 \sinh(qV\lambda/2kTd) \qquad (3)$$

where is the zero voltage intercept current, λ is the ionic jump distance with the other terms as given before. Fig. 70 shows that at 80 and 100°C the curves no longer can be described by the Schottky or Poole-Frenkel effects. If those two are hyperbolic sine relationships, then a plot of ln I versus V should produce a straight line at high voltages. The data of Fig. 70 were plotted on such a graph as shown in Fig. 71 for the two highest temperatures. Although some scatter exists,

Fig. 69. Conductivity of an 11,000 Å film illustrating three distinct regions. Region 1 is probably due to electronic conduction mechanisms, regions 2 & 3 are probably ionic.

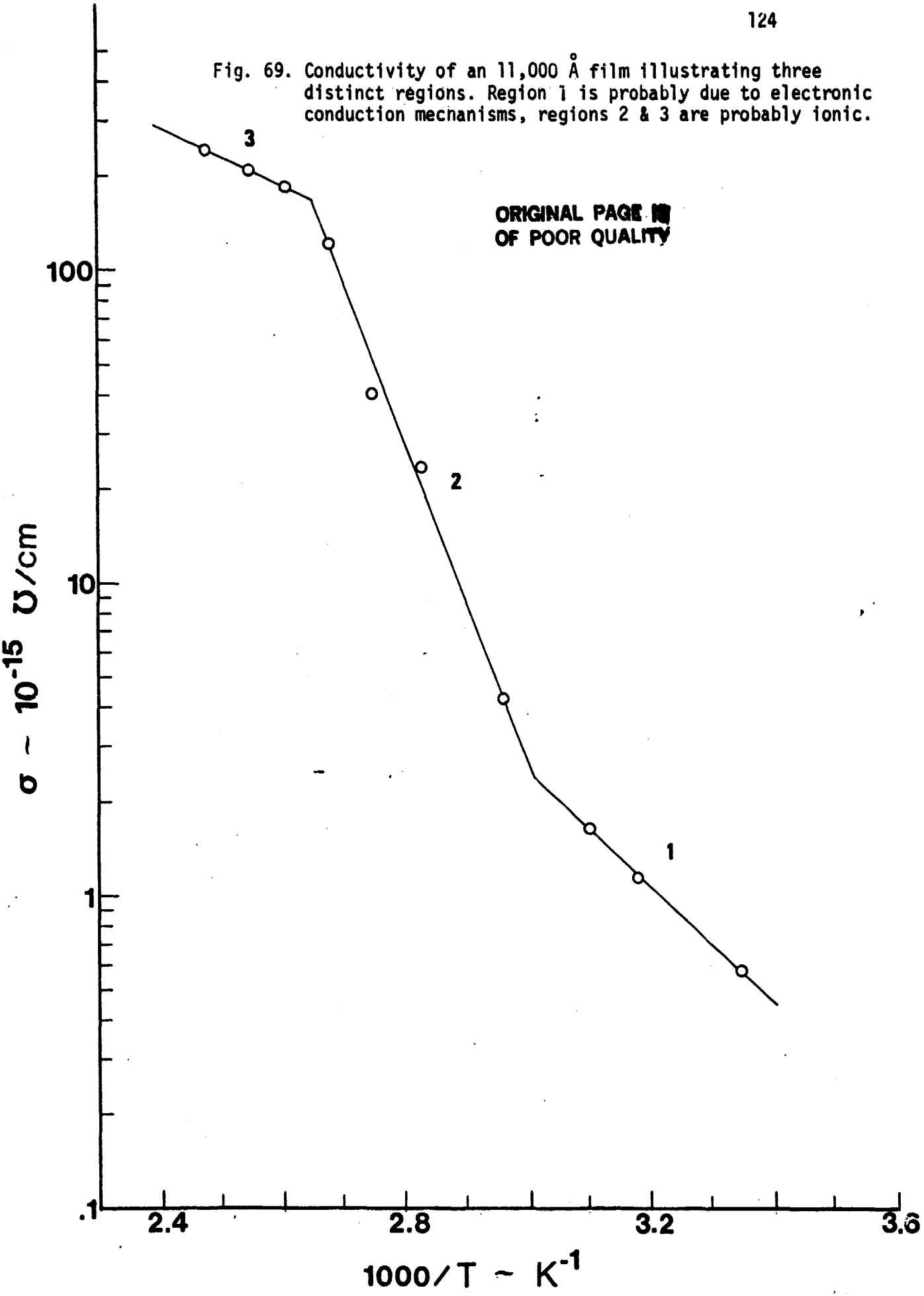


Fig. 70. Current-voltage curves of a 4,000 Å film at various temperatures. The change in conduction mechanism above 55 ° C is apparent from the changed slope of the curve.

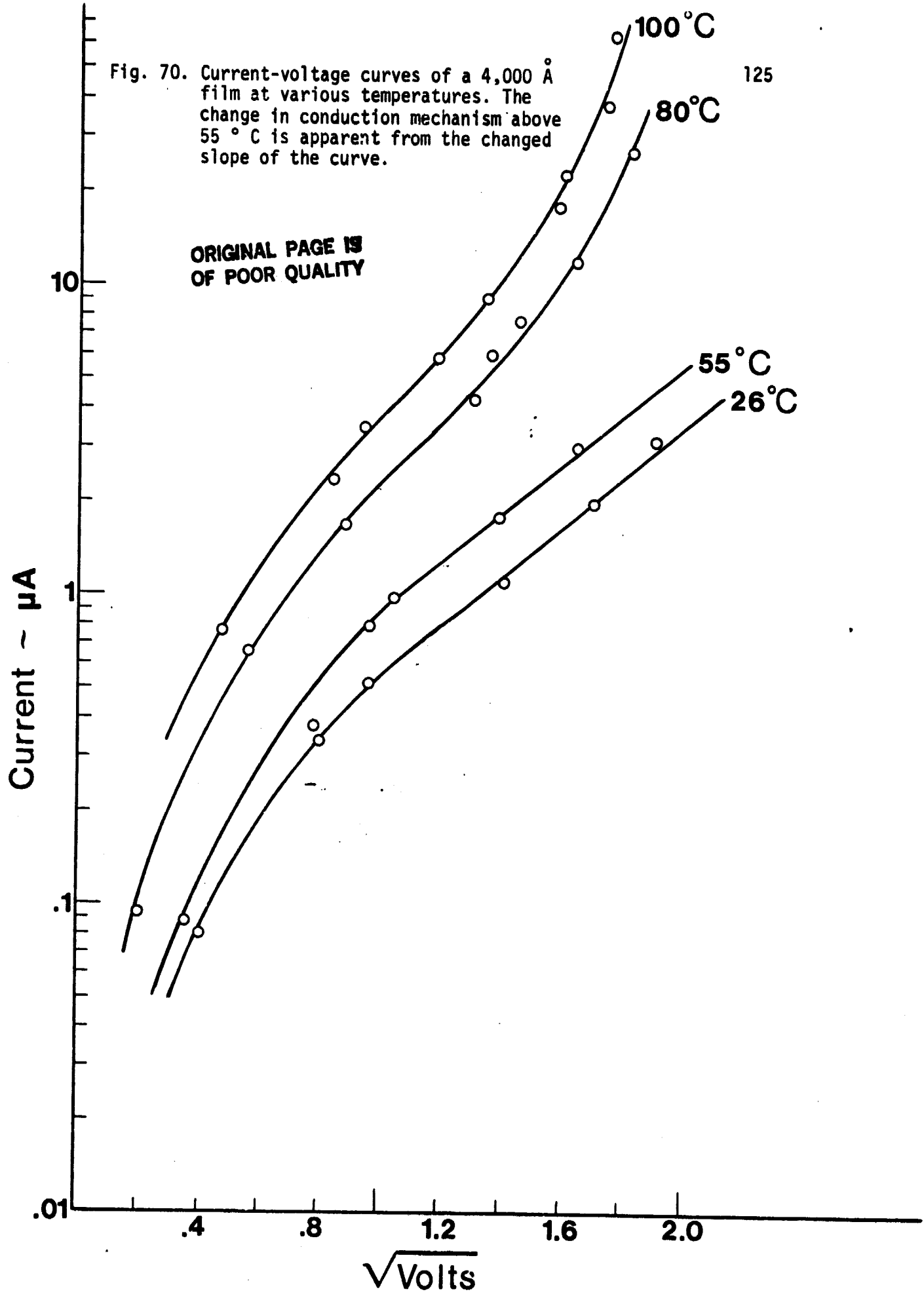
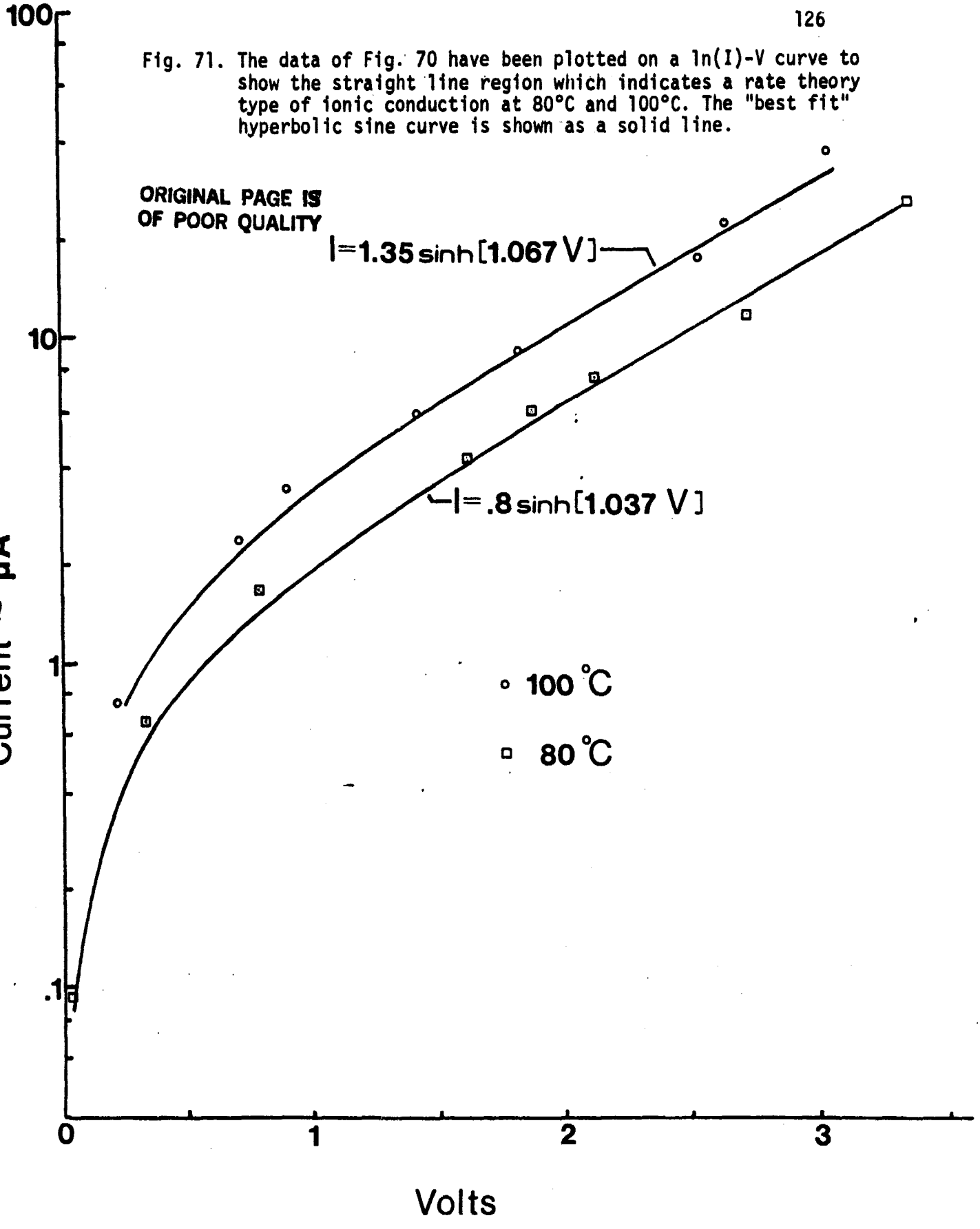


Fig. 71. The data of Fig. 70 have been plotted on a ln(I)-V curve to show the straight line region which indicates a rate theory type of ionic conduction at 80°C and 100°C. The "best fit" hyperbolic sine curve is shown as a solid line.



the data does form a reasonably straight line at voltages above 1.5 volts. From the slopes of those regions, the jump distance were determined to be 252 A at 80°C and 274 A at 100°C. Such an increase in jump distance with increasing temperature has been observed in polymers by other investigators. Using the jump distance data and the zero voltage intercept currents, the hyperbolic sine relationships were plotted in Fig. 71. The data points fit reasonably well over the entire range.

To help make certain that the higher temperature curves were not electronic conduction phenomena, they were treated as such and a determination made of the dielectric constant assuming Schottky or Poole-Frenkel mechanisms. Those data are given in Table VII. At the two lower temperatures, where electronic processes for conduction have been assumed, it can be seen that the dielectric constant determined by the Poole-Frenkel mechanism overestimates the measured value of 3.5 and thee value determined from the Schottky calculation underestimates the value. This is consistent with, although not independent of, the previous conclusion that the low temperature conduction was a combination of the two electronic processes. However, in the case of the two higher temperatures, both calculations yield dielectric constant values considerably below the value of 3.5. The conclusion is that the higher temperature region must be dominated by ionic conduction mechanisms.

Table VII. Dielectric constant estimated from the slope of the ln I versus $V^{1/2}$ assuming Schottky and Poole-Frenkel mechanisms. The measured value of dielectric constant was 3.5.

Temp.	S	PF
26 C	1.63	6.50
55 C	1.56	6.24
80 C	.46	1.84
100 C	.28	1.13